

Some Thoughts on Cold Electronics

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February, 2010

Introduction

A cold electronics design for the liquid argon TPC has many aspects that must be carefully examined. Important areas are the reliability of the components themselves, the impact on the physics performance of a component failure and the influence of the mechanical design on the electrical performance. These are also present in a warm design but the difficulty of modifying or repairing a system immersed in liquid argon means that extra care is required in the design and testing phase.

If one looks at inaccessible detectors such as the CDF and D0 silicon detectors or the D0 fiber tracker system, one finds that there are a number of channels that have failed. Also, the percentage of failed channels corresponds well with the fraction of the detector that is unrepairable. These facts indicate that we should put a lot of effort into making a robust, fault tolerant design.

Many detectors have either had performance problems or even failed because of mechanical features participating in the electrical circuits. With electronics now becoming inaccessible, it is very important to look at these details.

Design Constraints

There are three main parts to the front end electronics system: preamplifiers, analog to digital conversion and multiplexing. The multiplexing can be done either before or after digitizing so there really two possible systems. The cold-warm division can occur at each boundary or at the end of the system. Detector requirements significantly constrain these choices.

Since the drift time is of order 2 ms, there must be continuous digitization over this time period. Constant digitization is required for neutrino astronomy. The digitization rate used in the ICARRUS detector is 2.5 MHz with a 10 bit resolution. I will use this as the baseline in the discussion below.

A 2.5 MHz digitization rate probably rules out large scale analog multiplexing followed by transmitting the signals to warm electronics. Cable lengths may be as long as 25 meters so settling times off 50 to 100 nanoseconds or more are almost certainly required. This would restrict the level of analog multiplexing to only 2 or perhaps 4. Reducing the cable plant by perhaps a factor of 4 is certainly not a negligible change. But additional control cables as well as additional power and complexity will also be required. A proper risk assessment depends on the details of the design.

Digitizing without multiplexing just increases the cable plant without any real benefits so it is not worth considering.

From these considerations, the only two viable systems are cold preamps with direct connections to warm digitizers with the possibility of a small amount of analog multiplexing and cold preamps, digitizers and multiplexors. Note that a 10 bit digitizer requires more than 10 lines. The SVX2 chip has a highly optimized bus structure designed to minimize the number of signal lines. It requires 15 lines for 8 bits not including any power or grounds. Adding 2 grounds to the signal cable gives 19 total lines for a 10 bit digitizer. Thus, one has to multiplex by more than a factor of 20 to get a reduction reduction in cable count over straight analog transmission.

Design Details

Preamp

If we assume 5 mm wire spacing for all wires and diagonal wires at 45 degrees, we get 484 wires/meter for a set of 3 planes. If a preamp chip has 128 channels, then one chip would service 260 mm of detector. This is a good match to a circuit board but it means that one chip failure would put a large hole in the detector. A better method might be to have one chip for each plane. This would require almost 900 mm for 128 channels of diagonal wires which is a rather long board. Connections to the wires and differential contraction issues will require careful design.

A better method might be to use only 64 or even 32 channels per chip. This will drive up the chip cost but may make for a more reliable system with a more graceful failure profile.

Another issue with a cold preamp is the AC return path to the high voltage plane. This path is part of the preamp circuit so if it encloses a lot of high frequency noise sources, these may show up in the signal. the best method is a local capacitor that is directly connected to the HV plane. This would have to be in the liquid so it seems rather risky. A shorted capacitor would take out many channels. Good alternatives are not obvious.

Both CDF and D zero have had many power wire bond failures. A large fraction of the D0 failures are not well understood. D0 also has a large number of down load failures. D0 has used the SVX II chip in the fiber tracker where the electronics is readily accessible. The chip failure rate in that system is less than 2% while more than 10% of the silicon system is not working. This points to a large component of mechanical failures.

Some of the D0 power pads used double wire bonds. Very few of these have failed so one precaution is to use double wire bonds on all critical lines. D0 has also managed to use an alternative power path through the protection diodes in the chip. That is, when

the power wire bond fails, they power the chip through the readout and control lines via the internal protection diodes. It would be quite simple to provide a second power bus with a diode connection to the internal power plane. The secondary bus would be set at a voltage so that the diode drop will hold off power from the secondary bus unless the primary bus fails.

Finally, the chip design itself can be optimized for reliability. If the chip only has preamps, then the individual preamps can be made as independent of each other as possible. Extra metal layers can be used to build in local capacitance rather than relying exclusively on external components.

Cold ADC's and multiplexors

Multiplexing in the argon is significantly complicated by the requirement for continuous readout. Just digitizing for one drift period for accelerator based physics adds considerable complexity. The simplest method is to digitize all the data and send it all out by multiplexing the signals onto a single cable. The rate is limited by the bandwidth of the cable. D0 uses 3M pleated foil cable and achieves a data rate of 53 MHz for roughly 25 meters of cable. This is done by using both edges of the clock so the effective rate on the cable is only 26 MHz. Using both clock edges has proved to be quite difficult in practice so it is unlikely that the rate could be doubled. A factor of 20 multiplexing gives no gain in cable plant over direct analog transmission and requires 50 MB/s signal transmission (25 MHz on the cable). A 32 to 1 multiplexing requires 80 MB/s (40 MHz on the cable) which might just be possible. Cheaper cabling such as Spectrastrip twist and flat will have an even lower upper bandwidth. Serial cables such as cat 5 cables could go faster but these require multiple serial transmission lines and usually require data transmission protocols such as 8B-10B.

An obvious solution to the rate problem is to go to zero suppressed readout. Most of the detector has no signal most of the time. Since you have to add the channel address into the data stream, this requires either using 2 clock cycles to send one hit or else widening the bus by 6 to 8 bits. You only gain from zero suppression if you then increase the multiplexing rate beyond the upper limit of the cable for a complete readout of all channels. This are at least two issues with this. Given that events are localized, it is certainly possible that a large event or a medium event plus a cosmic ray will exceed the data transmission rate. This can be handled by time stamping the data and then putting the data into a large FIFO. Data is read out of the FIFO at a constant rate. Adding a time stamp adds perhaps another 8 bits to the data packet is now well over 20 bits which further increases the cable size. Note that reading all channels is necessary both for testing the hardware and for measuring pedestals etc. so even if pileup is a rare occurrence, some form of buffering is likely to be required. I think that the main issues are likely to be chip complexity and robust system design.

A second issue with high speed, highly multiplexed cable is the possibility of pickup by the detector itself. All of the above comments are based on single ended drive. CDF

could not readout and digitize at the same time unless they went to full differential drive. This will almost double the number of conductors in a cable. Any system will have several thousand cables all running in sync with a common clock. The design of the system to prevent unwanted feedback will be quite challenging.

Chip layout

One possibility for a preamp, ADC and multiplexor is to build the entire circuit in one chip. This certainly is the cheapest way to go but it is not the most robust design. A more robust one is to build the preamp as a separate chip. The preamp is then connected to two different ADC/multiplexor chips which are powered by separate power supplies. That is, the bus from the preamp chip would stop at two ADC chips. Each chip would have separate power and enable line so if one chip failed, one could simply switch to the reserve chip. Both chips would use the same output cable. The chip would need to be designed so that it did not load the cable if it was unpowered. This doubles the number of chips but the added cost may not be very large.

Summary

This note is an attempt to list some of the constraints that need to be satisfied for a cold electronics design. If CMOS technology can be modified to work at 90 Kelvin, then it is certainly possible to build TPC electronics that will meet the goals of the experiment. A non zero suppressed digital system does not appear to offer much of an advantage over direct analog transmission to warm digitizers. Local zero suppression has the potential to significantly reduce the data rate if one can develop a good design to solve the pile up issue.

History has shown that a large number of chips designed by the HEP community have errors in them. The only way to find these errors is extensive testing in a realistic prototype detector. As the chip complexity grows, the testing requirements grow even more. An ADC chip with zero suppression and multiplexing will require extensive tests in a prototype detector which has perhaps 5% to 10% of the channels of the final detector. This is likely to be a big effort.