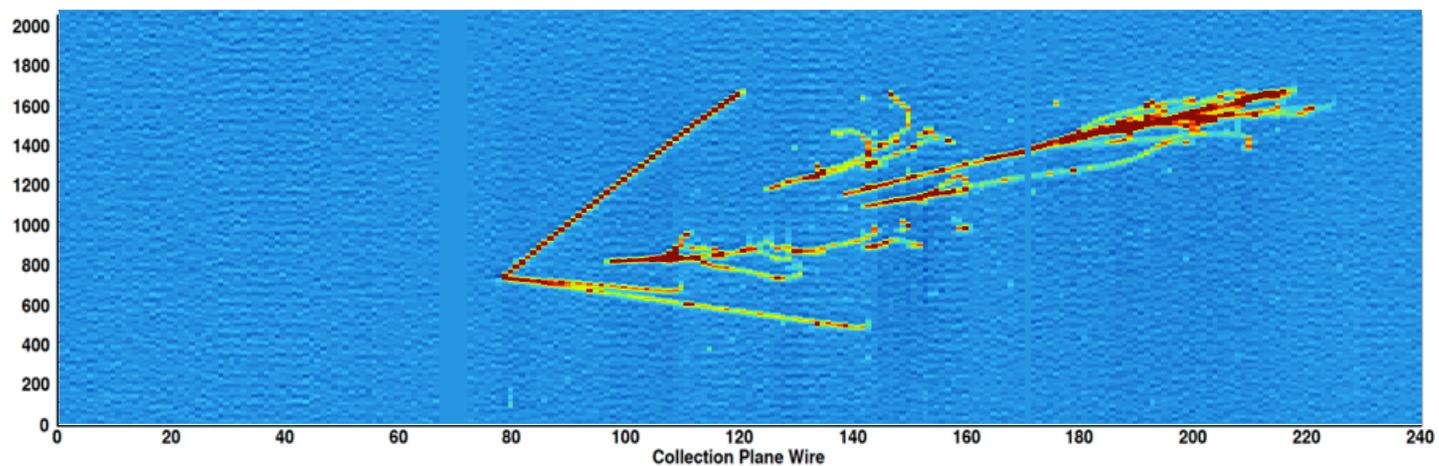


# Phase-1 MSU Cold Electronics

some questions

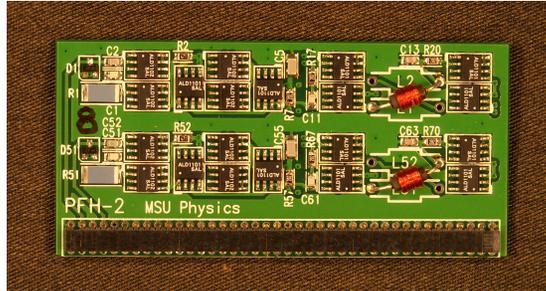
Carl Bromberg  
Michigan State University

ArgoNeut  $\nu$ - event with 4 photon conversions

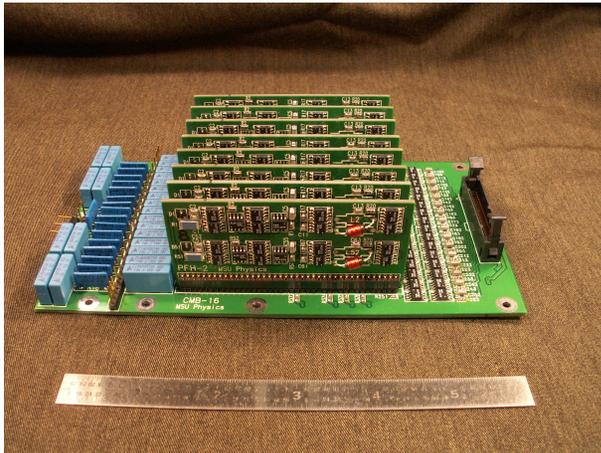


# MSU cold electronics components

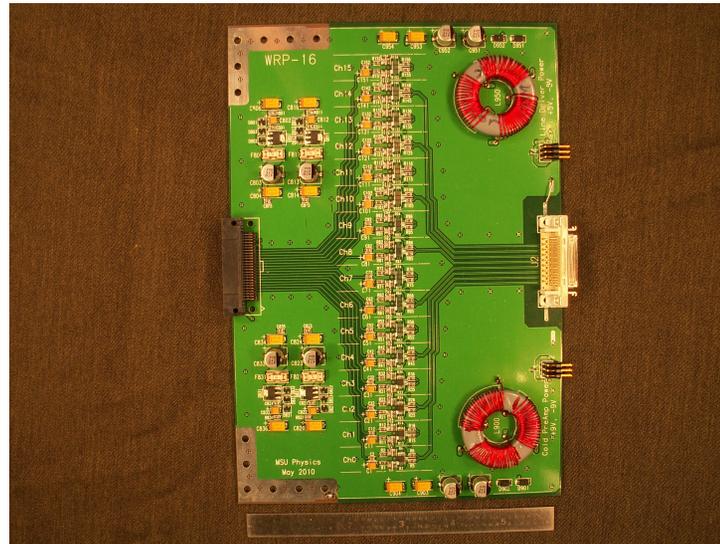
Cold dual-channel  
CMOS preamp hybrid



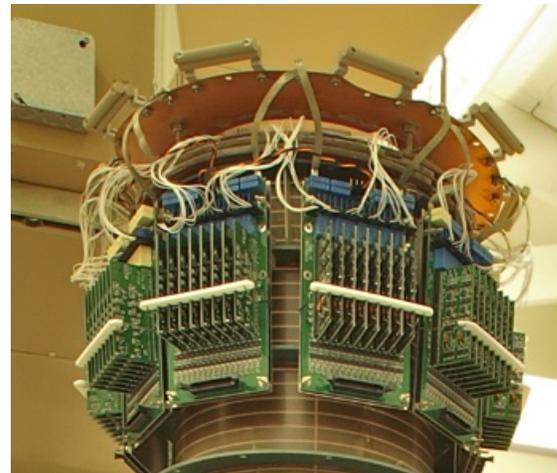
Cold motherboard with bias-V  
distribution and 8 dual preamps



Warm receiver, cable-driver at feed-through



Preamps on 2m Long-Bo



a) What does the improved signal/noise ratio buy us in terms of physics reach?  
Alternatively what are the current limitations of the MicroBoone electronics that we would be circumventing by switching to the MSU electronics?

- **Last question:** Indicates a misunderstanding of the situation:  
Alternatively? Switching? Circumventing?
  - MicroBoone electronics are NOT AVAILABLE. MicroBoone has to be successful in 2014 - LArIAT will be a diversion. Ask the PM!
  - MSU cold electronics has been available for 2 years, and is the ONLY cold CMOS electronics EVER to have readout a LArTPC.
  - For various reasons MSU cold motherboard must be the base for ANY cold electronics in Phase-1. MicroBoone motherboard will NOT work.
  
- **First question:** Physics reach of low noise cold electronics
  - Compton scattered photons generate low energy electrons well below 1 mip.
  - Low noise needed for EM showers and EM component of hadronic showers
  - In MC, remove all energy depositions below 200-keV and see what happens!
  - Also, S/N important if desired Argon purity is not achieved.

b) How does the noise floor and dynamic range of the preamps compare to the Microboone setup?

- In CMOS, MSU's cold preamp S/N cannot be surpassed!
- Dynamic range of the preamp is not an issue.
- What MicroBoone setup is that?

c) Ditto for the ADF2 digitiser

- ADF2 digitizer employs a 10-bit ADC. 12-bit NOT required
- If preamp gain set for RMS noise level  $\sim 1$  count, 1-MIP  $\sim 30$  counts.
- Collection plane pedestal 100 counts: 924 counts available = 30 MIPs.  
This is more than enough for the energies in LArIAT.

d) The 1Hz digitization seems to be a serious limitation, as it appears the rate in the TPC will be 4Hz. The minimum requirement should be full buffering of a spill. What is driving this limitation? Questions on this point:

Is this something that electronic engineers/ DAQ programmers from other institutions could help to fix?

What is the size and nature signal at the digitiser?

Is there something special about the ADF2 or is it possible to switch the digitizer to either an off the shelf model or some other university provided unit?

- Use of 400 ns sampling (1024 samples) increases readout rate to 2 Hz.
  - Full buffering of 4s spill? Are we looking supernovas?
  - Triggered readout of 350 microsecond drift-time is what is needed.
  - Other institutions? Got any suggestions? Full documentation on web.
  - Further increases in readout rate possible but issues:
    - More Bit3/PCI paths (Bit3 no longer produced)
    - Zero suppression algorithm in FPGA -- could be important for LBNE. Might be of interest at MSU or elsewhere – expensive labor – got the \$?

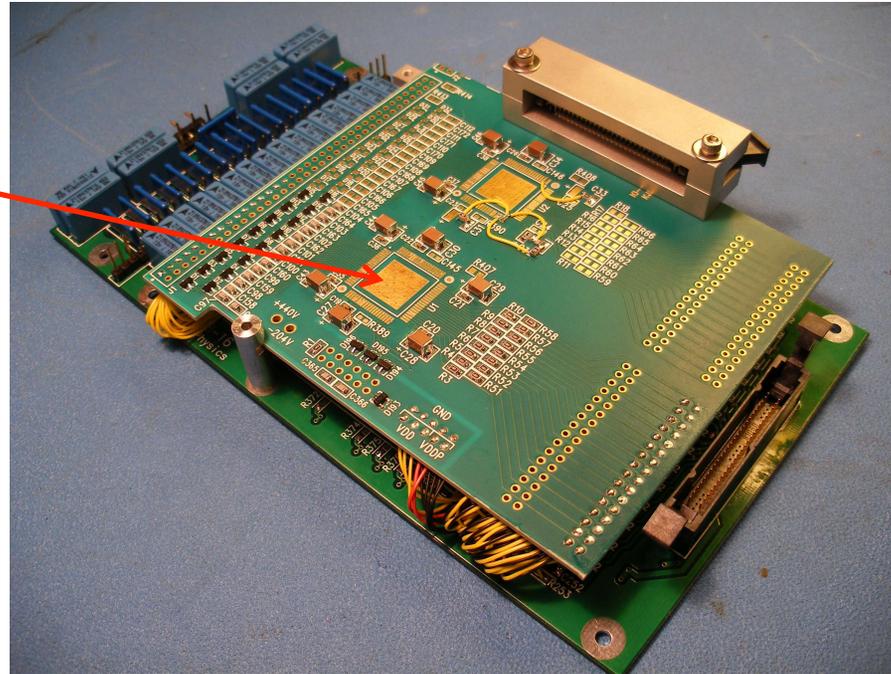
e) Does the choice of cold vs warm amplification stage have any impact on trigger rate?

– NO

# BNL ASIC will be tested in Long-Bo this Fall

Modification of MSU motherboard  
with BNL – ASIC mezzanine card

ASIC goes here



- Test sanctioned by MicroBoone PM to obtain muon data in LArTPC
- Replaces one MSU preamp motherboard for the Long-Bo tests
- Will test full range of ASIC parameters – determine S/N.
- Can revise motherboard for direct ASIC mounting in the future.