

# LArIAT trigger system

Mike Kordosky

# What do we want it to do?

- Find cases where a particle enters the detector through the vacuum can (or cosmic for calib)
  - instantaneous coincidence of beamline & other signals
- Protect against overlap
  - earlier/later particle through the can  $|\Delta T| < T_{\text{drift}}$
  - earlier/later particle on the periphery  $|\Delta T| < T_{\text{drift}}$
  - later particle  $|\Delta T| < T_{\text{drift}}$
- Prescaling (needed?)
- Incorporate PID into trigger
  - CER easy, TOF harder

# Requirements

- Input: analog signals from counters (TOF, CER, WC, VETO, COSMIC) and TPC PMTs
- Actions (*in order of development priority*):
  - 1 coincidences & anti-coincidences between any of the above (programmable)
    - A To trigger
    - B to veto
  - 2 pre-scaling different triggers
  - 3 TOF in the trigger
- Output:
  - 1 logic signal → TPC digitizers
  - 2 counts, analog waveforms, TDC, QDC → disk

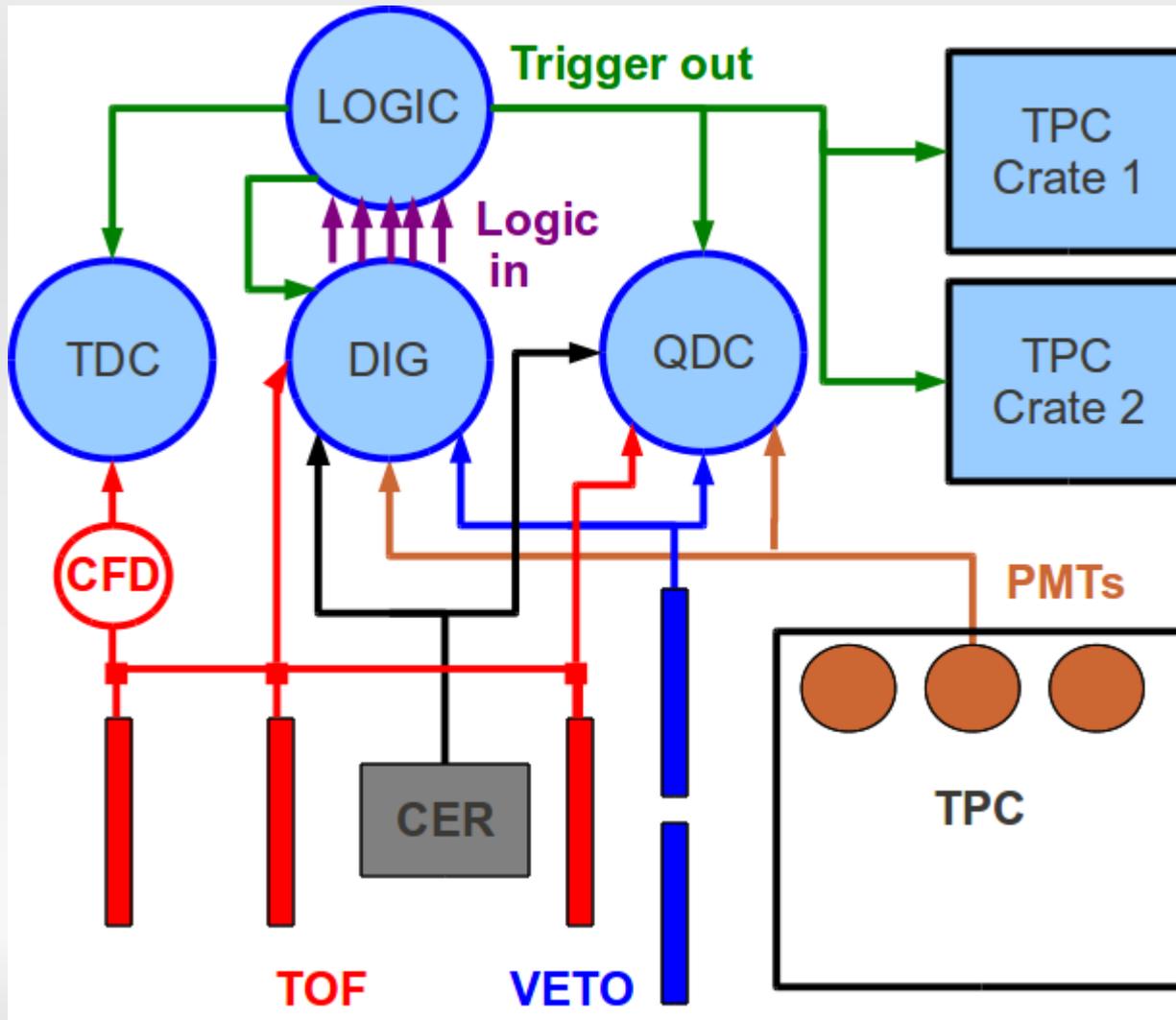
# Trigger decision

- Look for *out of drift* veto conditions
  - if yes, start a veto counter VCTR, updating continuously
- Look for interesting coincidences COIN
- If !VCTR and COIN
  - start a counter → drift time
  - monitor for *in-drift* vetos
    - if so, set VCTR, abort
  - no vetos → end of counter, send stop to ADF2

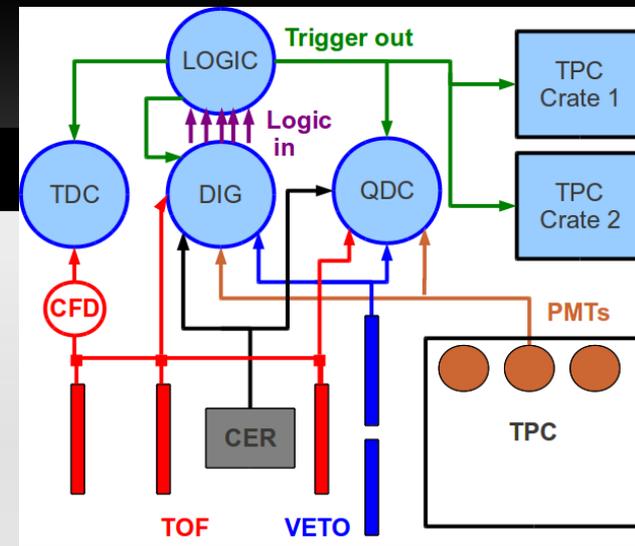
# Sample Patterns

TOF1	1	-	1	etc...
TOF2	1	-	-	
TOF3	1	-	1	
CER	0	-	-	
VETO1	0	1	0	
VETO2	0	-	0	
WC1	1	-	1	
WC2	1	-	1	
WC3	1	-	1	
WC4	1	-	1	
PMT1	1	-	-	
PMT2	-	-	1	
TRIG?	1	0	1	
VCTR?	0	1	0	

# Conceptual overview

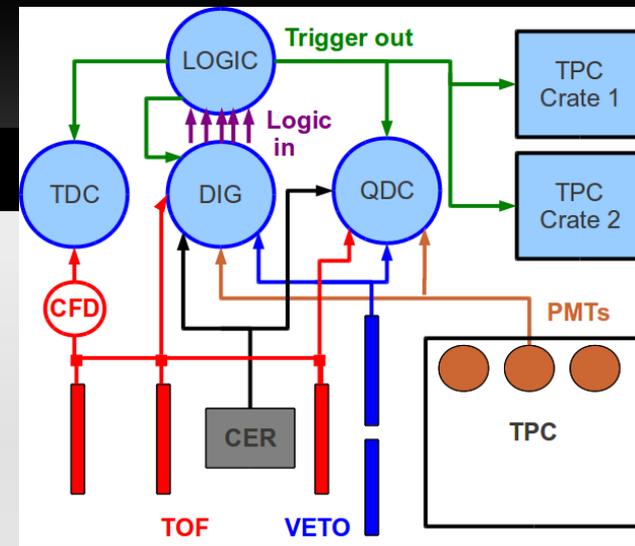


# LOGIC



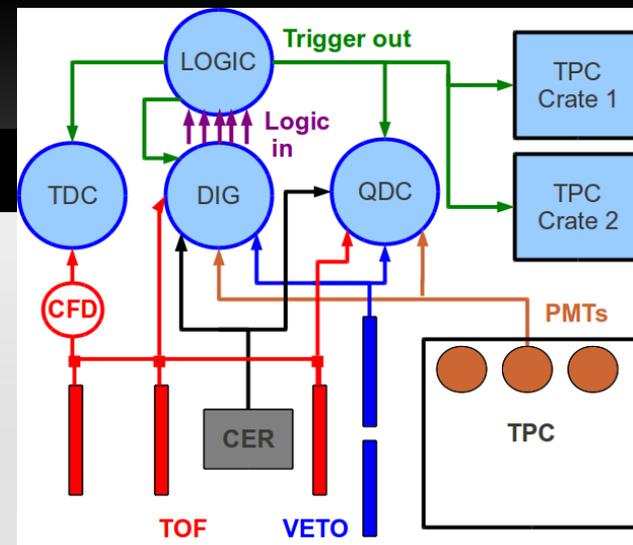
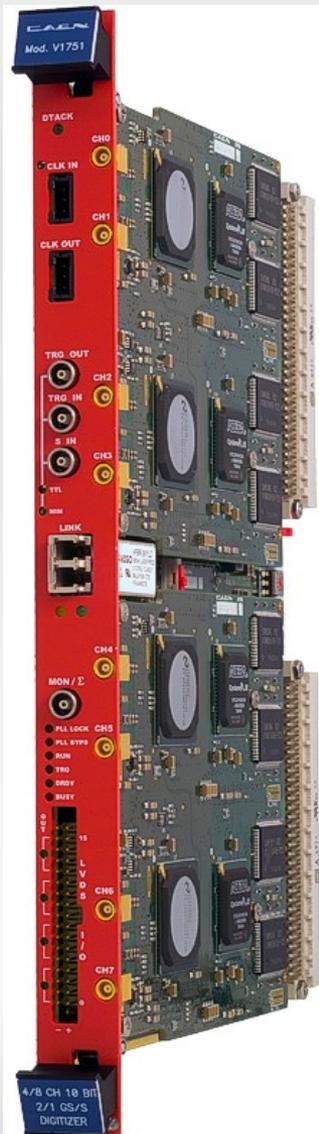
- CAEN v1495
  - Altera Cyclone chip
- At W&M now
- 64 ECL inputs
- 8 NIM inputs
- 32 ECL outputs

# LOGIC



- WM undergrad working on FPGA programming
  - training: WM electronics and JLAB SULI
- FPGA based bit pattern generator available
  - electronics lab project last semester

# DIgitizer



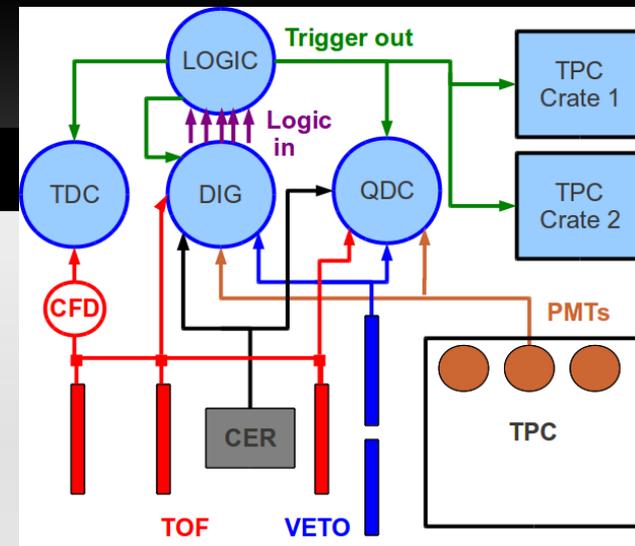
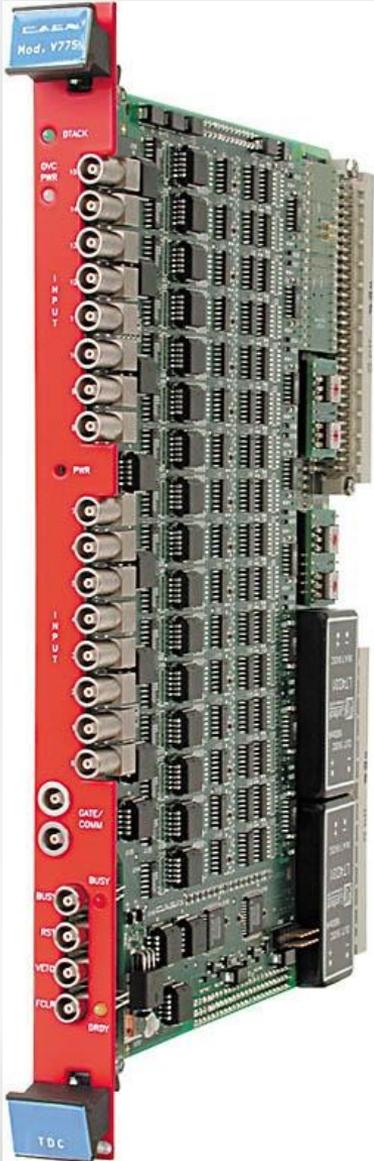
- CAEN v1751 or similar
  - 8 chan, 10bit @ 1Gs/s
- Yale: 1 on order
- Takes analog signals, produces logic.
- v1720 at WM
  - 8 chan, 12 bit @ 250Ms/s

# Bare bones!

- I did some work on my v1720 in my copious free time last summer
- The vendor libraries are very bare bones.
- Found myself immediately implementing, e.g.,
  - structs to hold config information
  - `config(struct& s) → writes to registers`
- Have a different undergrad working on the UI side of things → but low duty factor

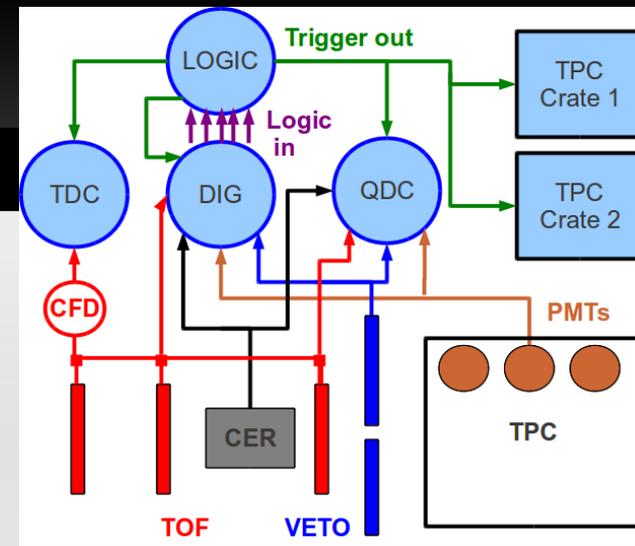
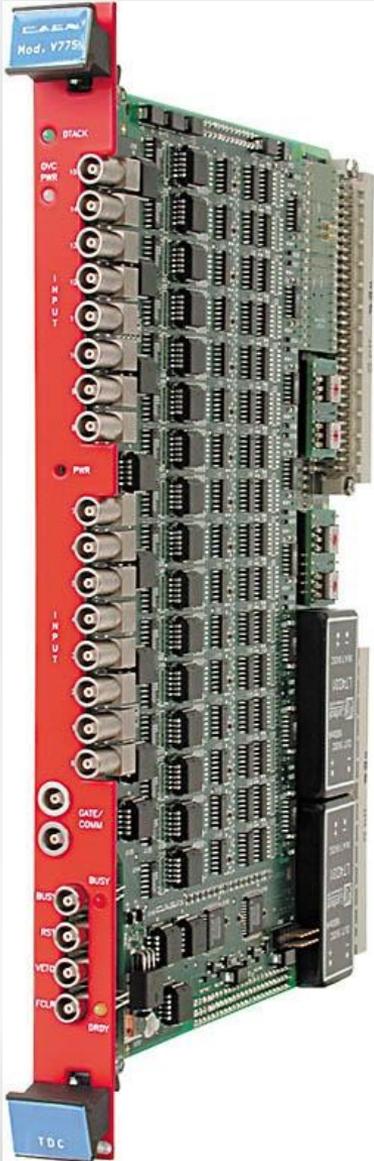
**Anyone Have  
Some Code??**

# TDC



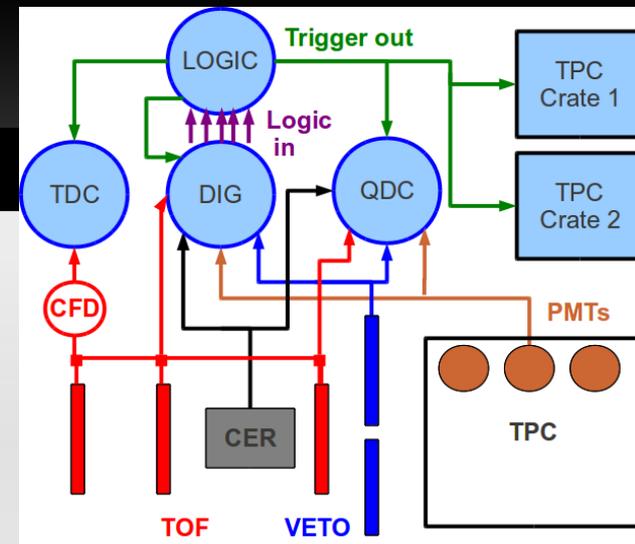
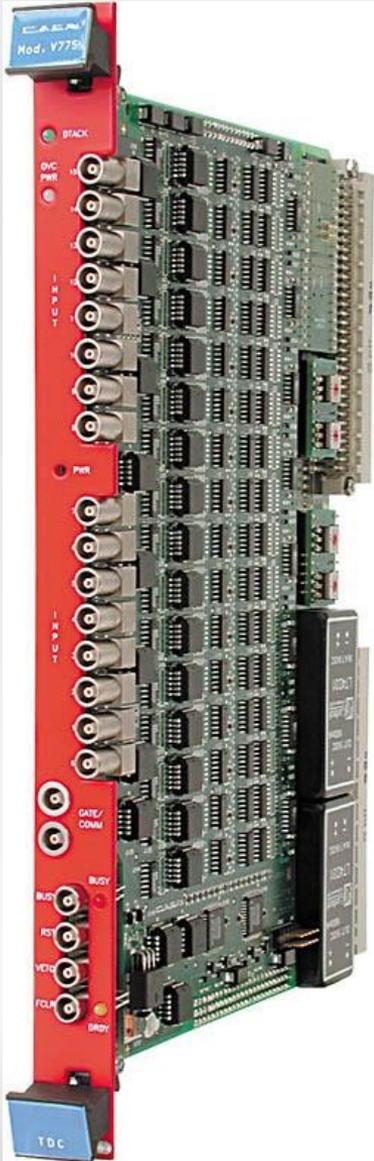
- CAEN v775 or similar
  - 16 chan, 35ps LSB
- 1 at WM now
- Needs logic signals
  - CFD or equiv

# TDC



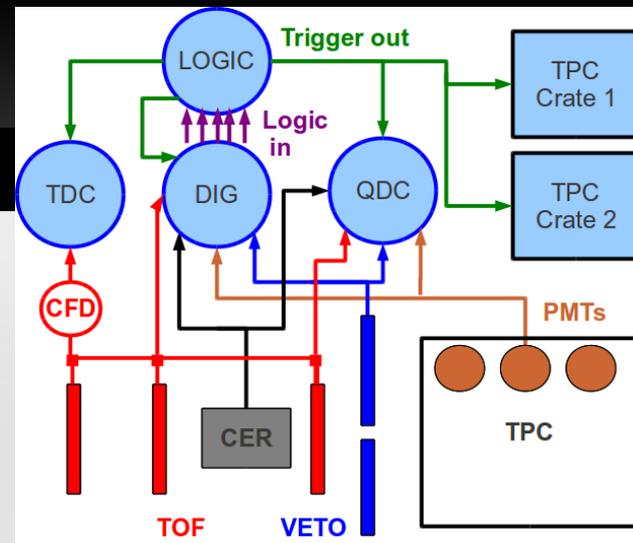
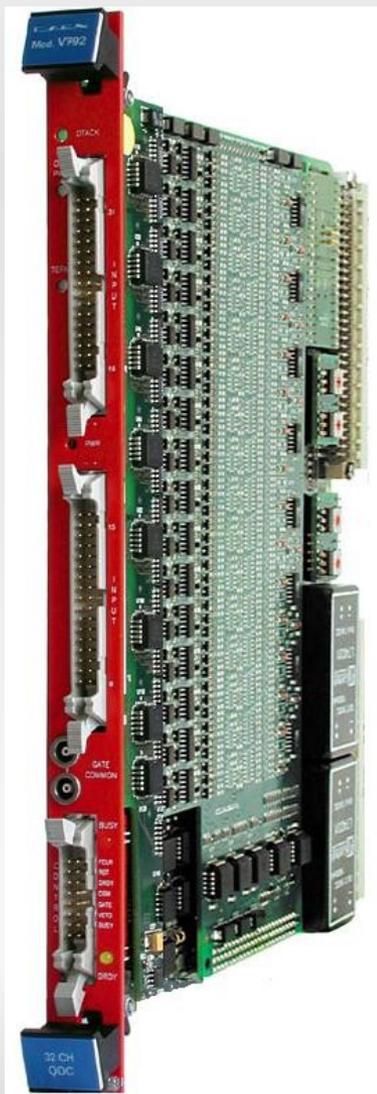
- Works off of common start
  - coin of CFD signals
  - Stops need (low dispersion) cable delays
- common stop mode avail.
- digitization  $\sim 3 \mu\text{s}$  (ok)
- no trigger out (bad)

# TDC



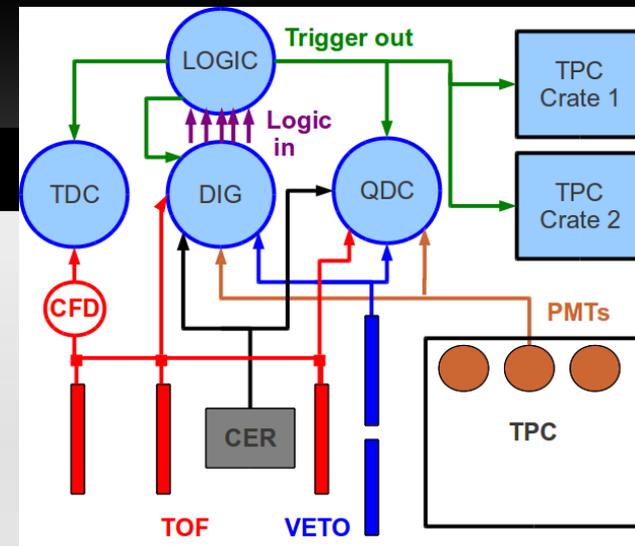
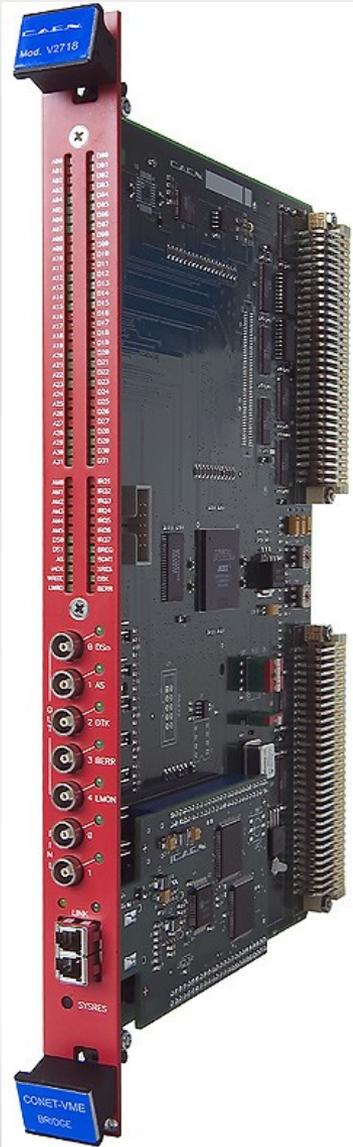
- Workable solution
- I have CFD and other NIM stuff → better, PREP
- Q: can a 1Gs/s or 2Gs/s digitizer perform as a ~100ps TDC?
- May need to send BUSY to LOGIC

# QDC



- CAEN v792 – 1 at WM
- 32 channels – LEMO converter boards in hand
- 12bit, 100fC LSB
- No experience with it yet
- Not clear we need this

# Controller



- CAEN v2718, PCIe optical
- Can raise IRQ on host PC
- Have 1 at WM
  - Haven't used yet → PCIe interface needs new computer
- Experience with v1718

# Needed items

- **Additional digitizer**
- NIM and VME crates at FNAL
- NIM modules
  - CFD, level trans, scalars, fan-in/out, linear translator, amps (maybe)
  - for testing: discr, logic, gate/delay
- **Computer for FNAL (full width PCIe x8,x16)**
  - alternative MVME5500?
- All detectors! I have nothing!

# Counters

- I think we need the following:
  - 3 TOF counters
  - logic pulse output from the WCs
  - A CER counter to tag electrons. Maybe only used for beam characterization.
  - VETO counters to cover the front of the detector
- I think we could use:
  - cosmic ray counters
  - downstream muon counter

# PID in the trigger?

- electrons via CER are easy
- TOF is hard:
  - you can do TAC but there is no logic in that TDC module to select certain time ranges (aside from zero suppression)
  - and there is no trigger output
  - So, must TAC, then communicate to CPU which considers, sends VME trigger → not ideal
- I think CAEN v1290 has these features.
  - but, is it really important?
- Silver bullet module from surplus?
- A bit more thinking. Possible clever solution.

# Momentum in the trigger?

- Disclaimer: I wish we could have a beam where we could *set* the momentum!
- Momentum based trigger:
  - Only way I can think of: feed WC digital pulses into the logic unit
  - 64 input channels, some expansion possible
- Then, magic occurs!
  - logic unit determines the momentum!
  - Maybe a LUT? Some simple “good enough” computation?
- Let's table this → bigger fish to fry

# Relation with TPC DAQ

- Initially, would like to keep separate
  - eases development and commissioning
  - loooong time between spills to match up data
  - Trigger DAQ enabled by TPC DAQ (TCP sockets or some such?)
  - don't have strong feelings here
- Will need to sync clocks in some way
  - Both systems reset at “Warning: extraction” and run free for 4 sec?
  - One system digitizes a clock from the other?

# Software

- CAEN vendor libraries are bare bones
  - Higher level code for digitizers helps a bit
  - But, if we want to control other cards, and use IRQ, lower level CAENComm library is recommended
  - But if you want to talk to the controller directly: CAENVMELib
- No trigger-DAQ framework
  - Was thinking of calling C code from python
  - Python: gui, config files, could call root, sockets
  - Any code I can repurpose / reuse?

# Wanna get involved?

- WM will deal with the logic module
- WM will manage the trigger DAQ
- Areas of work – people needed:
  - configuring and controlling different modules (writing higher level code)
  - structure of the DAQ
  - output format. Direct to root? Conversion program?