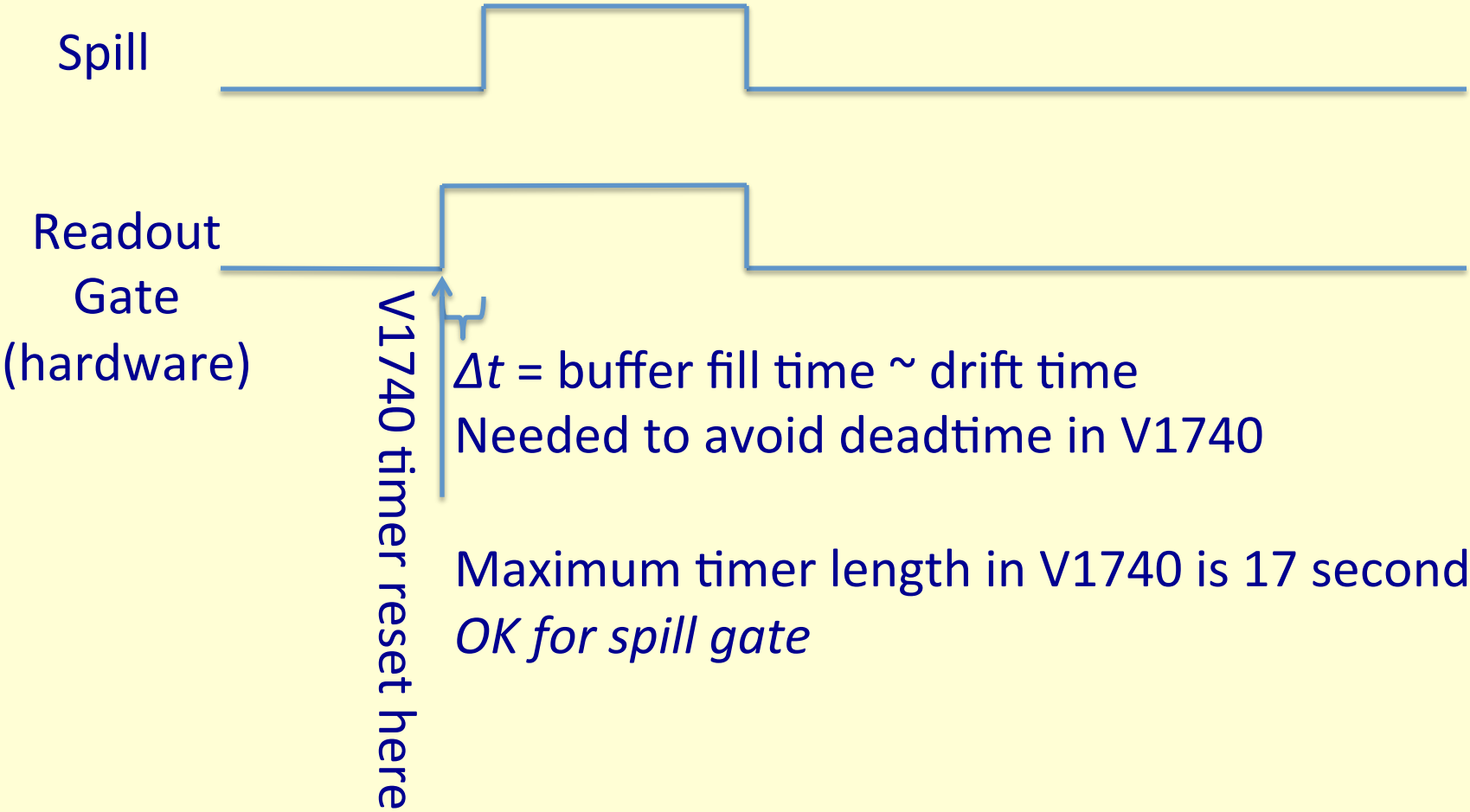
LArIAT Spill Readout Timing Remarks

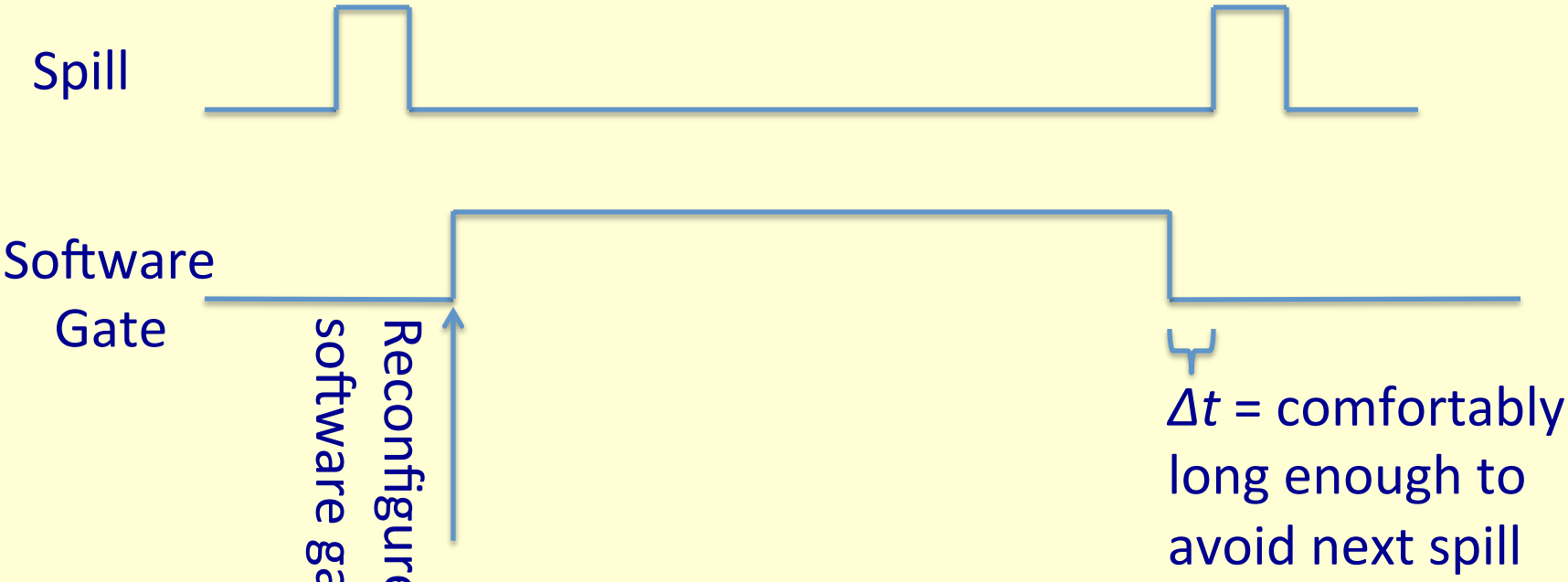


Δt = buffer fill time ~ drift time
Needed to avoid deadtime in V1740

Maximum timer length in V1740 is 17 seconds,
OK for spill gate

LArIAT Inter-Spill Timing

V1740 cannot run both hardware (front panel) and software gates at once



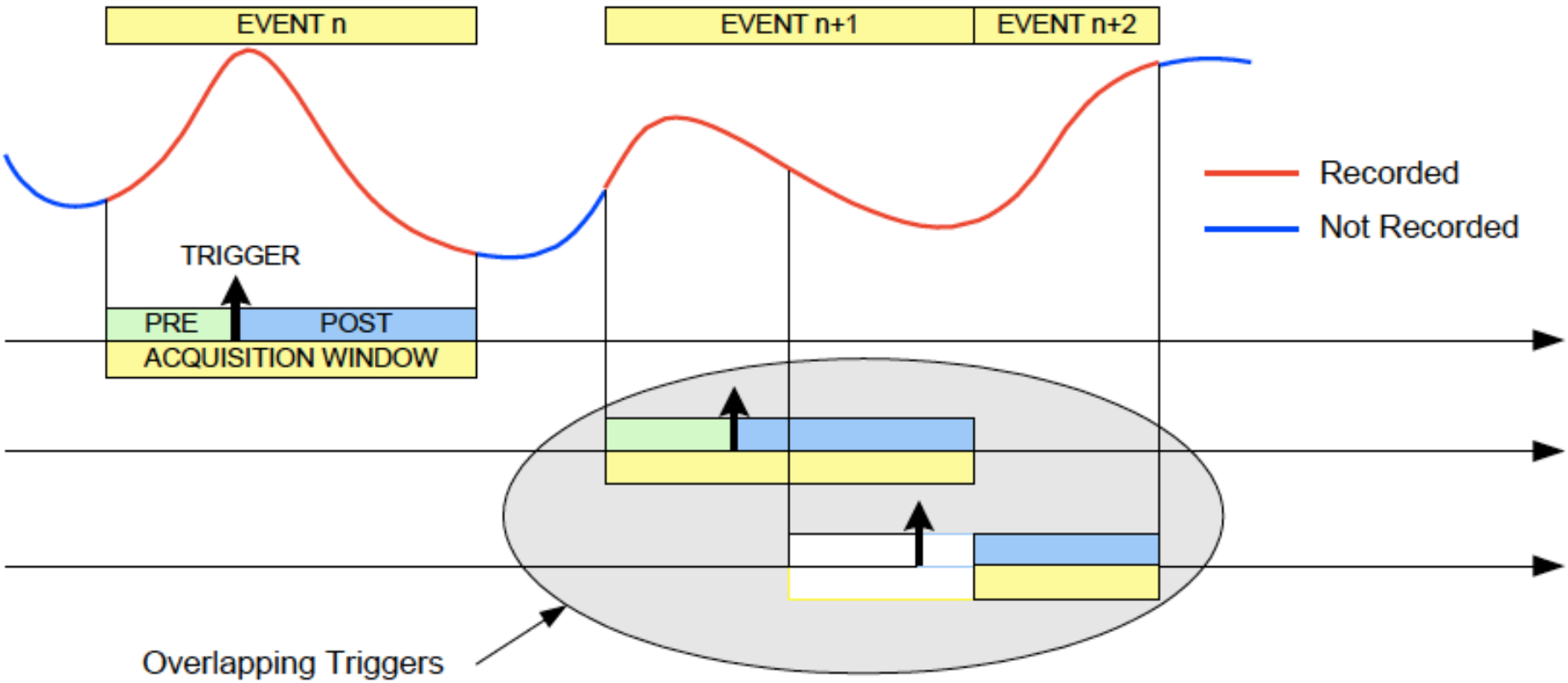
V1740 maximum timer length is ~ 17 seconds, inter-spill time ~56 seconds

Do we need to correlate TPC inter-spill triggers with other detectors?

Interesting LArIAT TPC Readout Option

V1740 can run "deadtimeless" with overlapping triggers enabled

Event matching would be necessary offline & have variable size events



Do we want to use this feature?

Only useful if post-trigger samples N>0

Fig. 3.3: Trigger Overlap

LArIAT TPC Buffer Options

Table 2.3: Output Buffer Memory block division

CODE	Nr. of blocks	Samples per Block (1 ch.)
0000	1	192K
0001	2	96K
0010	4	48K
0011	8	24K
0100	16	12K
0101	32	6K
0110	64	3K
0111	128	1536
1000	256	768
1001	512	384
1010	1024	192

Larger number of samples than the nominal 1000

LArIAT Clock Issues

Need to discuss and decide clock issues

- How stable does it have to be?
  - V1740 needs < 100ppm short term jitter
  - I have not found one that stable yet
- How well do we have to know the frequency?
- What about long term drift?
- Should we have a common clock for all systems?
- Do we need to record the frequency value periodically?
- Should we derive from the machine clock?
- What do the wire chambers currently use?

Can meet after this meeting to talk…