LArIAT V1740 TPC Readout Status

CAEN provided new "Decimation" firmware to slow down the effective sampling clock this week:

- Can reduce 62.5 MHz clock by 2^n where n=0…7
- With internal clock, attractive periods are 128 *ns*, 256 *ns*, maybe 512 *ns*
- Has desired averaging feature: all ADC readings in span are averaged to provide final value & useful for PMTs (verified)
- Can read out while buffers are being filled (also verified), simplifies and speeds readout
- May have additional V1740 soon, but no promises and change in final delivery date
- External clock still has problems, cannot PLL (previous positive report tricked by failover to internal clock, pby)

LArIAT Readout Status, all detectors

- Still not clear how many PMT channels will be present and how many need to be read out, fast and slow
- We now have "pseudo-integrating" slow sampling V1740 firmware, may be OK for some
- TPC and Wire Chambers are set
- Who needs to use the 16 spares V1740 channels?
- Does anyone need the spare V1751 channels?
- What information needed from TOF?
  - Up stream – down stream (yes)
  - Pulse height? Absolute time? Resolution?
- We need the interested parties to meet again to hash out these details, say in the new year

V1740 External Clock Observations

- Found HP 8082A pulse generator OK at 50 MHz
  - 50 MHz: ~ 1 in 1000 jitter (OK)
  - 62.5 MHz: ~ 1 in 100 jitter, much worse
- Testing <u>without</u> decimation
- Clock never appears at front panel clock output
- At 50 MHz (20 *ns*) V1740 quickly loses PLL and does not function, ignores triggers
- At 62.5 MHz (16 *ns*) readout progresses, but PLL flag is off
  - Suspect fail-over to internal clock
- Consulting with CAEN, but…
- Good chance we will have to use internal clock, daisy chained through 8 boards with delays timed in carefully
  - Limits us to 256 *ns* sampling period with 2^3 decimation
  - Need specific CAEN approved daisy chain cables
- Today engineering communiqué indicated external must be submultiples of 125 MHz (!) contradicting docs (!1)