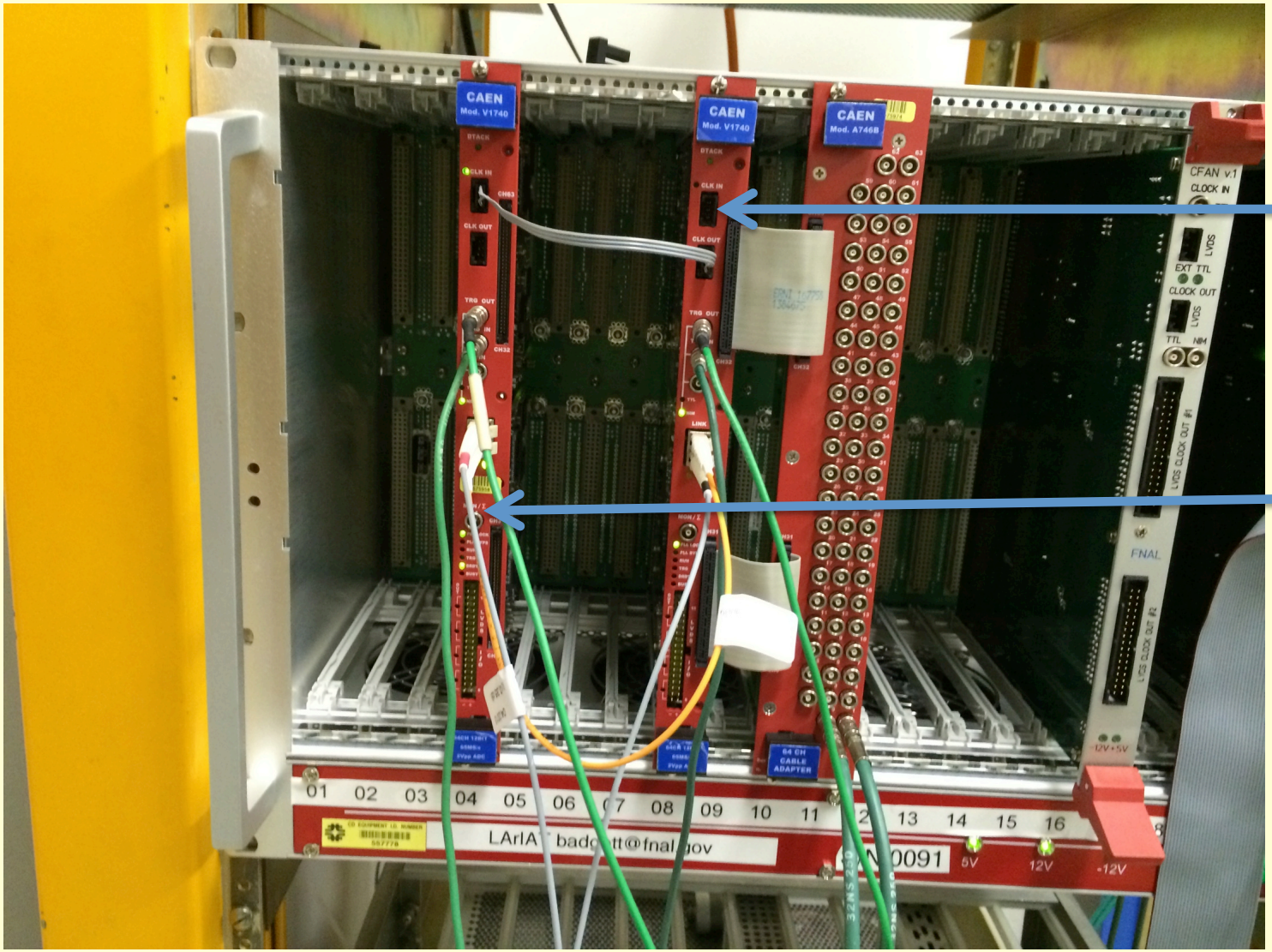
LArIAT V1740 TPC Readout

Second V1740 arrived last week



Clock Master, with internal clock

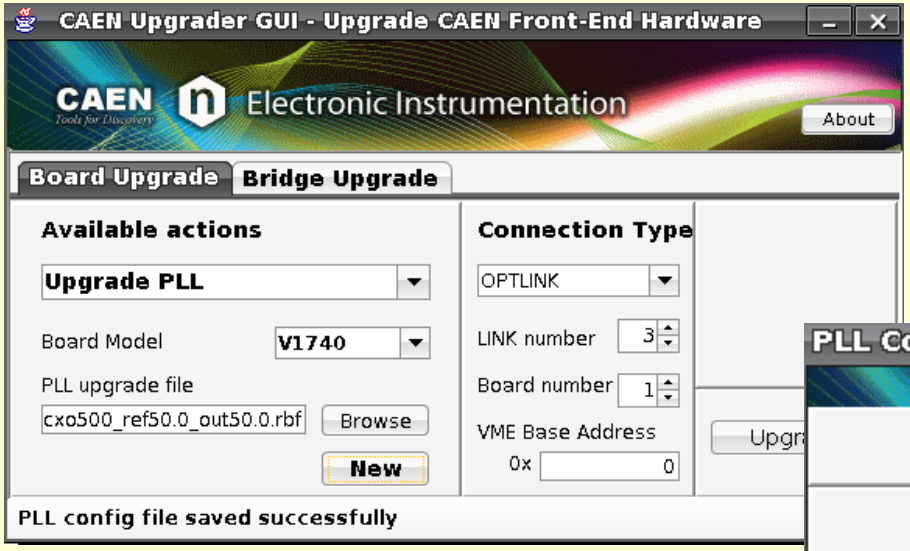
Clock Slave, with external clock, daisy chained

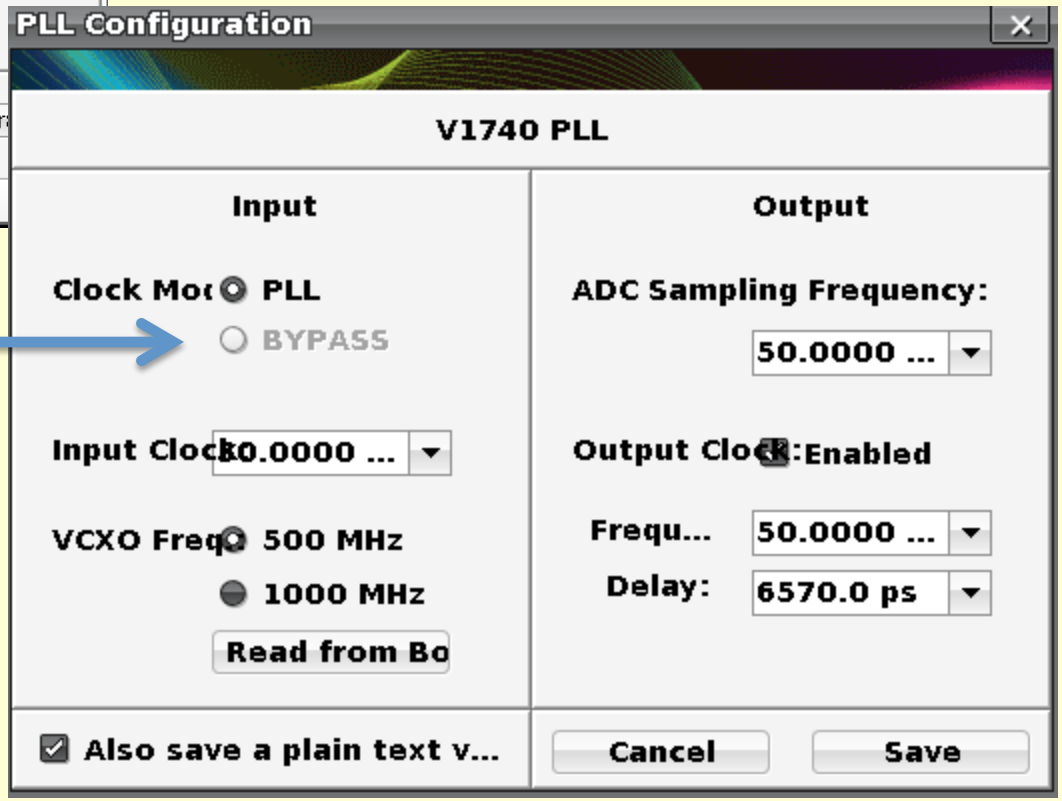
LArIAT V1740 Synchronization

Prior to synchronization, have 6.7 ns phase offset

LArIAT V1740 Synchronization

Use CAENUpgraderGUI to reprogram PLL clock settings





Note clock bypass mode option is disabled!

LArIAT V1740 Synchronization

Add 6.57 ns offset (quantized delay)
Synced to within ‘scope resolution

Jitter, both clocks:
8 ps / 20 ns

Limited by ‘scope 350MHz

LArIAT V1740 Synchronization

Possible V1740 sampling periods
Internal base clock is 500 MHz
Sampling frequency must be sub-multiple

500 MHz / n, where n = 8...16

			xDecimation			
MHz	n	ns	2	4	8	16
62.5000	8	16	32	64	128	256
55.5556	9	18	36	72	144	288
50.0000	10	20	40	80	160	320
45.4545	11	22	44	88	176	352
41.6667	12	24	48	96	192	384
38.4615	13	26	52	104	208	416
35.7143	14	28	56	112	224	448
33.3333	15	30	60	120	240	480
31.2500	16	32	64	128	256	512