

LArIAT TPC Digitization Options



Possible V1740 sampling periods

Internal base clock is 500 MHz

Sampling frequency must be sub-multiple

Time consuming to change frequency

Let's choose
this one

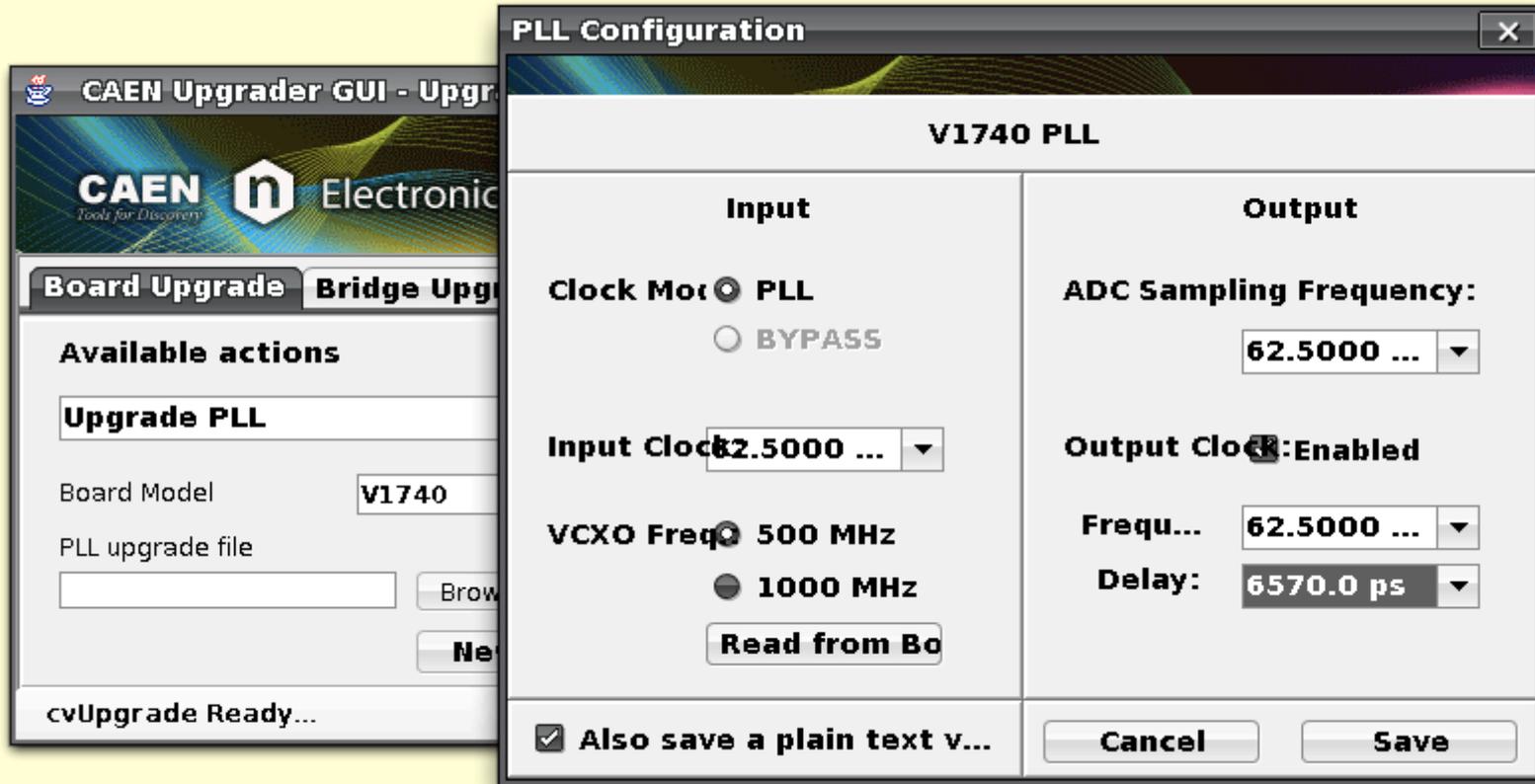
500 MHz / n, where n = 8...16

MHz	n	ns	xDecimation (up to 256)			
			2	4	8	16
62.5000	8	16	32	64	128	256
55.5556	9	18	36	72	144	288
50.0000	10	20	40	80	160	320
45.4545	11	22	44	88	176	352
41.6667	12	24	48	96	192	384
38.4615	13	26	52	104	208	416
35.7143	14	28	56	112	224	448
33.3333	15	30	60	120	240	480
31.2500	16	32	64	128	256	512

LArIAT TPC Readout Clock Options



Choosing most obvious 62.5 MHz settings
Approved by CAEN

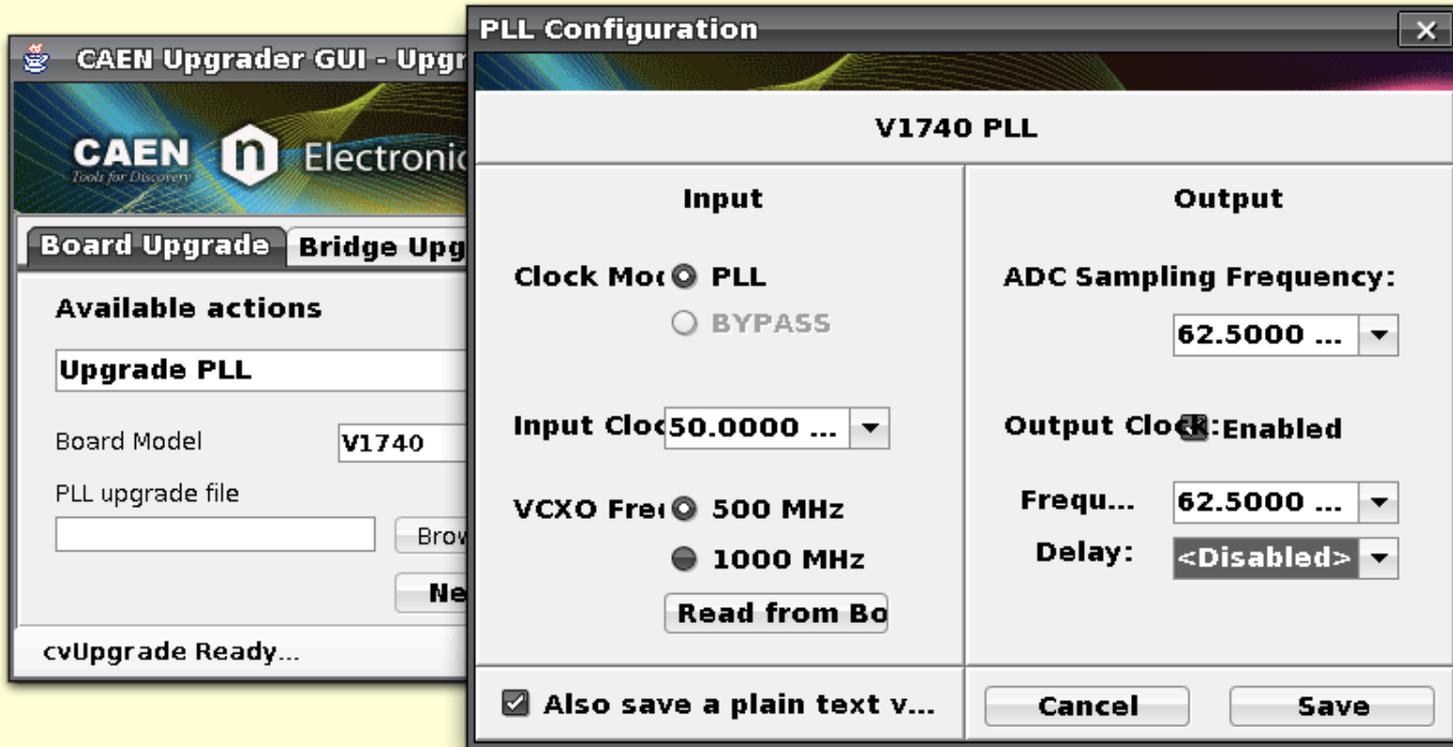


Input and output and sampling clocks 62.5 MHz
But even Master V1740 cannot lock PLL
Boards down the daisy chain malfunction strange ways

LArIAT TPC Readout Clock Options



CAEN Advises using 50 MHz input and output clocks
Sampling clocks stays at 62.5 MHz



All eight boards in clock chain lock their PLLs
...but clock delay correction is too long

LArIAT TPC Readout Clock Options

Smaller frequency clock needs 14.4 ns delay

Maximum delay in CAENUpgraderGUI is 9.8 ns



Paola and Marco (CAEN) investigating...

LArIAT TPC Readout Issues



Over the weekend ran ~ 1.5 days before crashing

Next run ran ~15 minutes before crashing

Rate 15 minutes – several hours

Two mysterious crash modes:

1. Run ends when all eight V1740s report CAEN_DGTZ_CommError
 - suspecting A3818 (PCI interface in DAQ computer) common problem
2. Run simply ends with no error or indication of signal received, no core file produce
 - A “kill -9” would do this
 - or an exit(0) call in CAEN code (quiet failure?)
 - Both cases will most likely need CAEN help
 - Another mysterious feature: Often after power cycle, firsts communications result in error; next time OK