

TPC update

Cinco de Mayo 2015

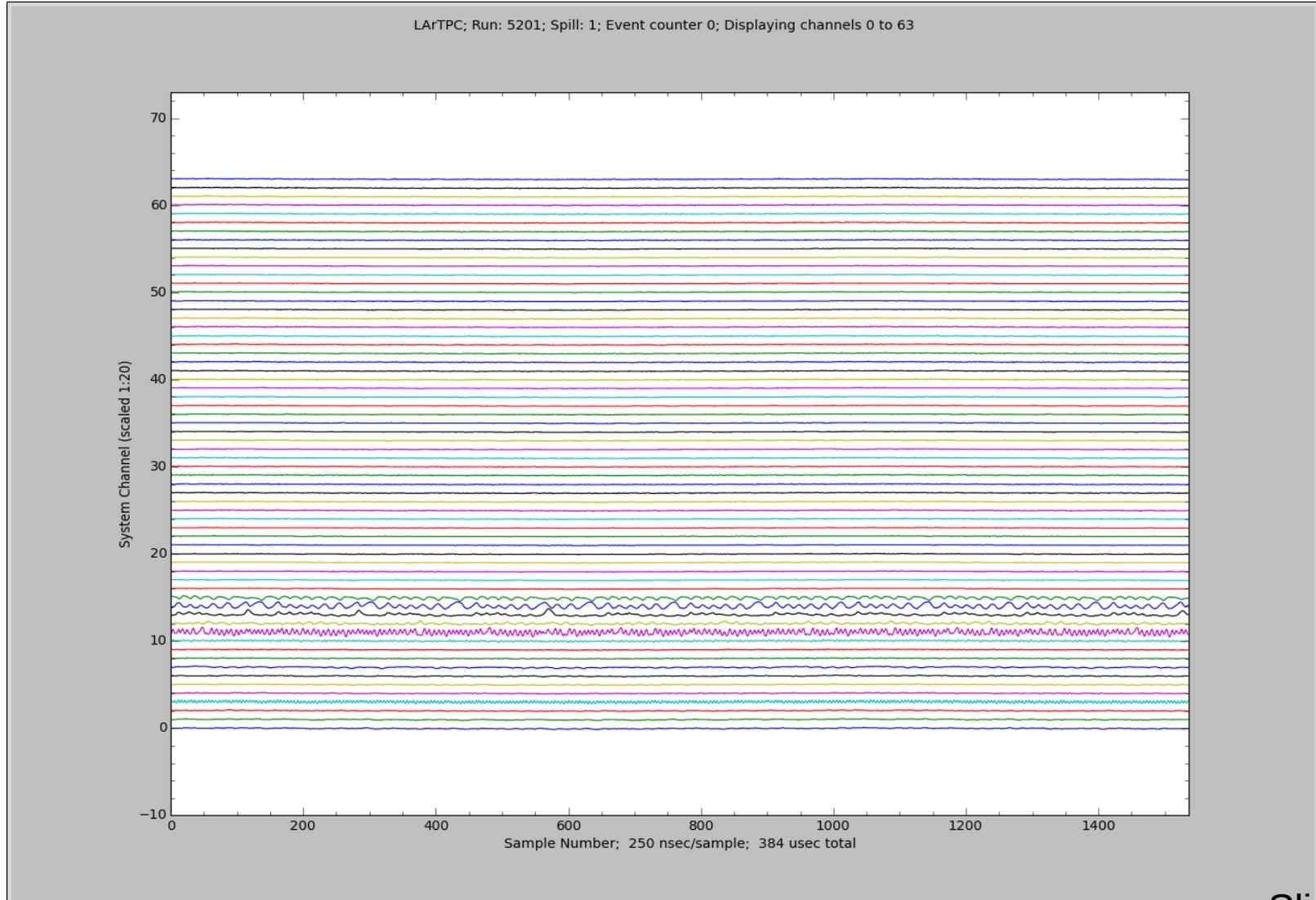
Dean Shooltz, Carl Bromberg

Now that the champagne corks have landed...

A few problems to address:

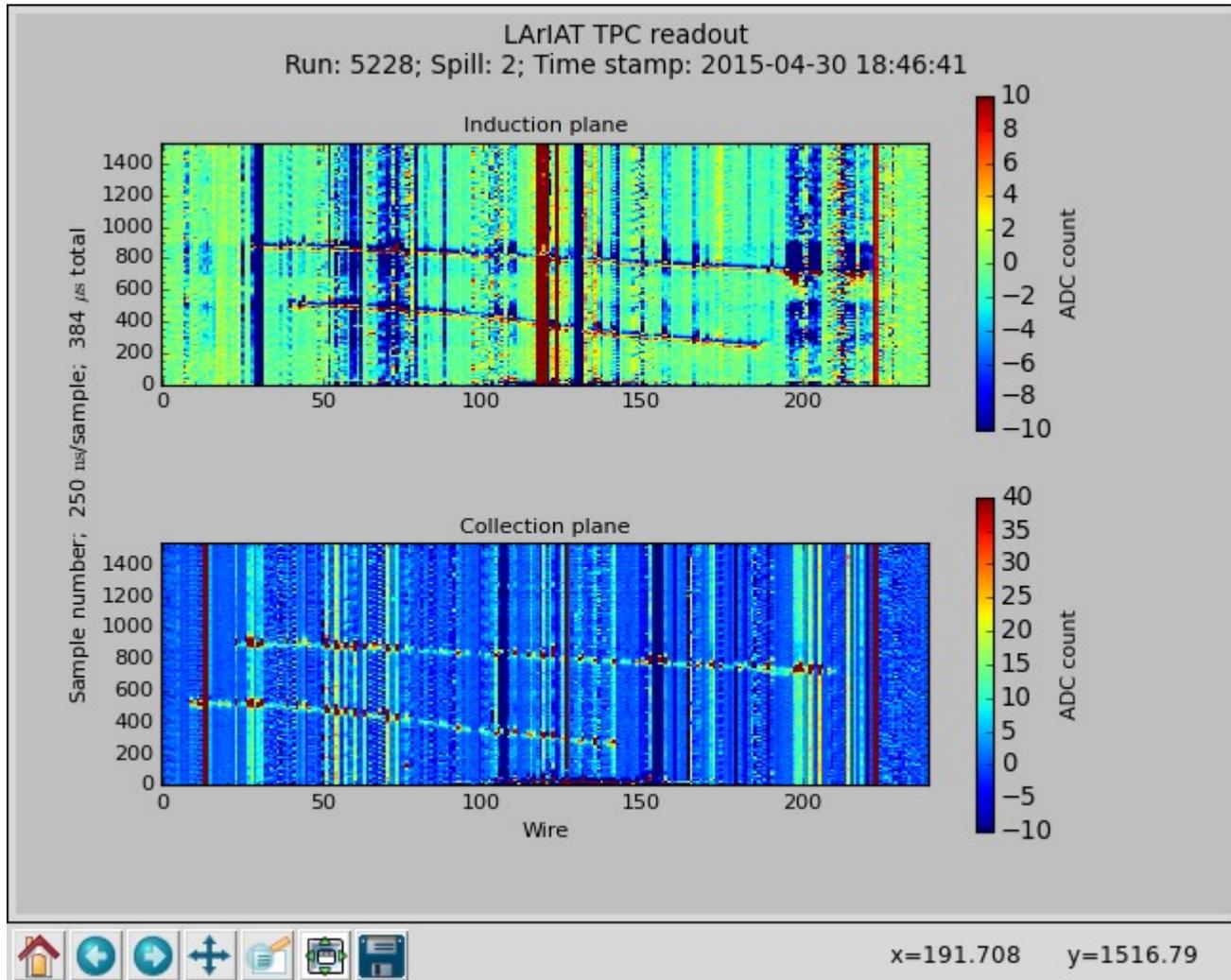
- (1) ASICs seem to enter a state with strange baseline noise
- (2) Signal amplitude seems too low
- (3) Small amount of cross-talk (ground bounce) on I-plane

- Elog 2441 CAEN traces from 480 wires look good
- Elog 2442 Bias voltage is turned on
- Elog 2444 New noise signal is discovered (look at traces 0-15):



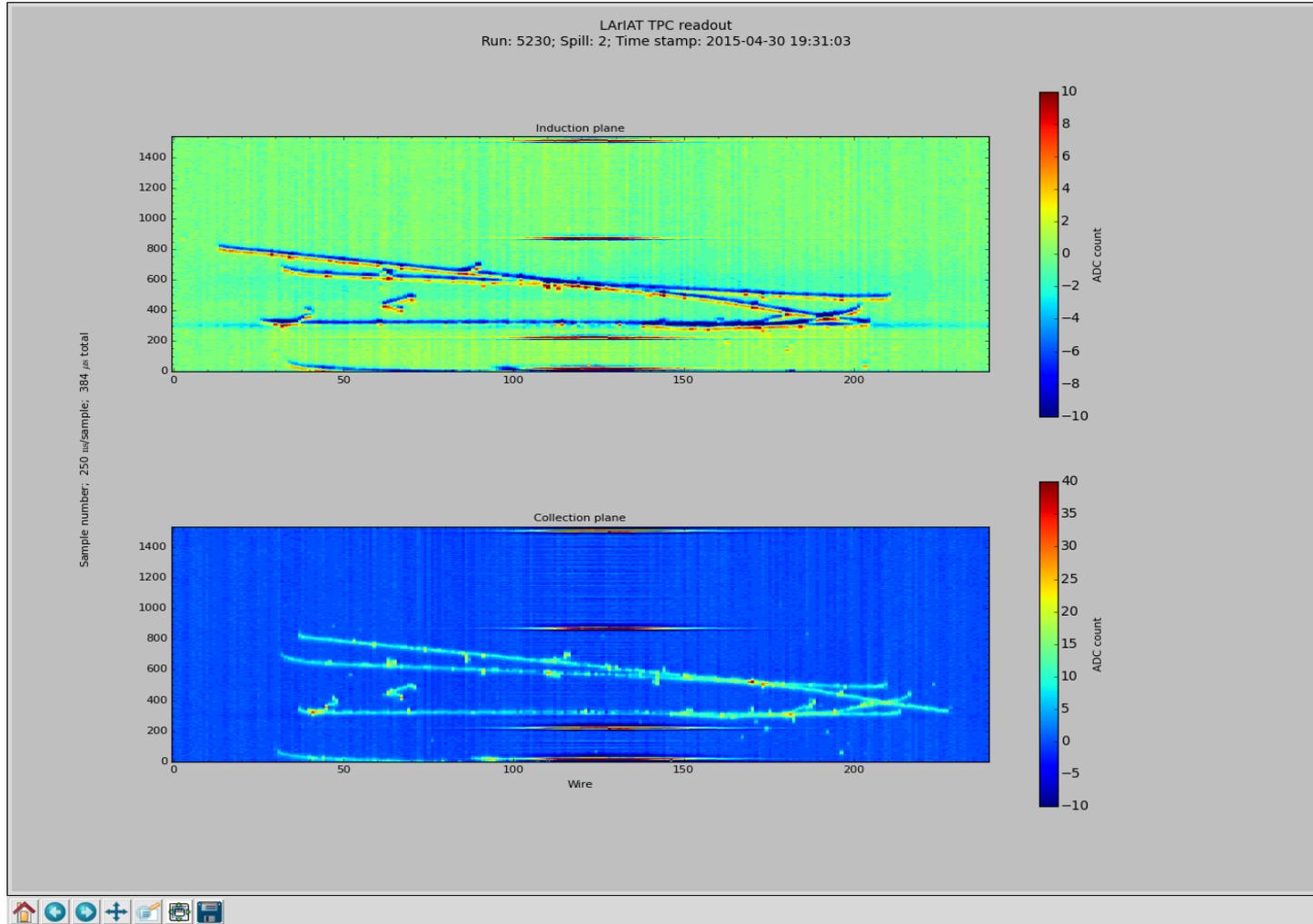
Event view of many ASICs with the strange baseline noise problem

Elog 2499- just before power cycle



Elog 2500 – just after ASICs power cycle

The power cycle seems to have fixed the ASIC problem



Characteristics of the newly discovered noise signal:

Appears to occur at the ASIC level.

Cycling the ASIC RESET lines does not alter the noise.

Only solution found thus far: power cycle the ASICs.

First time course after a power cycle: Elog 2517 (Thanks shifters!)

2 am 4 ASICs with problem

3 am 4 ASICs with problem

<...cryo fill happens here...>

4:12 am 10 ASICs with problem

4:46 am 12 ASICs ~

5:33 am 12 ASICs ~

6:39 am 12 ASICs ~

7:41 am 14 ASICs ~

The ASIC problem can evolve rapidly. Does it correlate with LAr manipulations?

A second time course of ASIC behavior is on going:

I have visually inspected all event displays in the Elog and noted the number of ASICs with the weird baseline noise problem.

There is no record in the Elog of any power cycle during this period.

Elog 2577 2015-05-01 12:41:53 Power cycle the ASICs (t=0)

Elog 2564 2015-05-01 14:04:48 ASIC #0 has the problem

<...many entries...>

Elog 2716 2015-05-04 09:47:54 ASIC #0 has the problem (t=69 hours)

Elog 2764 2015-05-04 18:27:40 ASICs #0, #27 have the problem (t=78 hours)

Elog 2818 2015-05-05 13:40:50 ASICs #0, #27 have the problem (t=97 hours)

This time course shows a far less frequent occurrence of the problem.

Could this problem be related to the environment inside the cryostat?

LAr levels?

Bubbles introduced during LAr fills (mentioned as possible in Elog 2551 by Russ)?

Possible solutions to the problem with the ASIC weird ASIC baseline noise problem

Keep monitoring- maybe this will simply go away (not satisfying)

If this is rare enough just make a CA for power cycling
(current situation, last power cycle over 97 hours ago...)

Install remote control for the TPC power
(Discussions ongoing)

Install remote control of ASIC power at the WRD-48 level (48 channels at a time)
(more work, finest granularity solution, can control through the Teensy interface)

Amplitude of the TPC signals

We expect 3.5 fC fo charge per wire per MIP

At highest gain the ASICs should develop 25 mV/fC

We expect about 87 mV signals per wire per MIP

The analog signal path from ASIC to CAEN has gain = unity
(designed that way, and verified yesterday at MSU)

The CAEN digitizers have 2 V p-p span, 12 bits

Expect 1 ADC count for each 0.488 mV at the input.

Thus we expect to see roughly 180 ADC counts per MIP.

However, we see only about 10% of this amplitude for cosmics.

Could this be due to no configuration of the ASICs?

(default state is all zeros in config bits, meaning lowest gain and tightest filter)
(thus weak signals)

Solutions for the signal gain problem

If we need to raise the gain in the analog system the best approach is to change two resistors in each channel of the D2S card.

With this change we should be able to raise the gain by a factor of up to 10 or more. (that claim needs to be tested).

Labor estimate: 480 channels, two SMT resistor changes per channel
So 960 changes at the component level.

That would require a minimum of two days (maybe longer) and a decent work environment (static-safe work bench, SMT rework tools, workbench, good lighting).

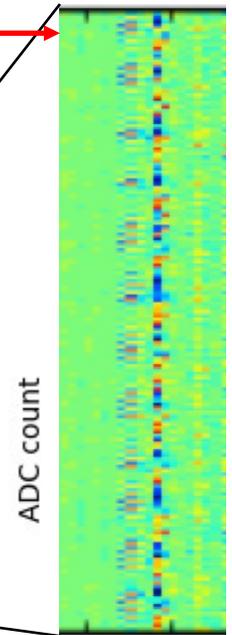
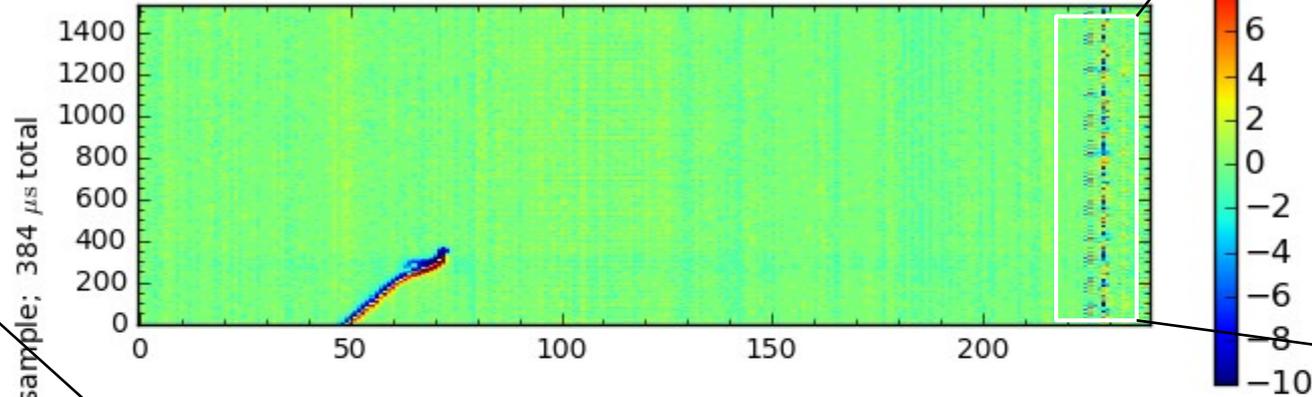
I am available until May 18th - after that I will be at CERN for most of summer.

Slide 1 of 2 from Carl illustrating / summarizing the current issues with TPC readout

Same pattern?

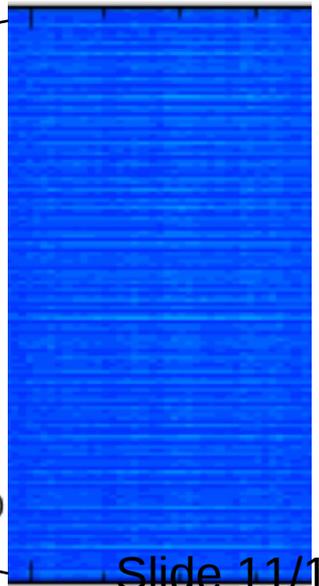
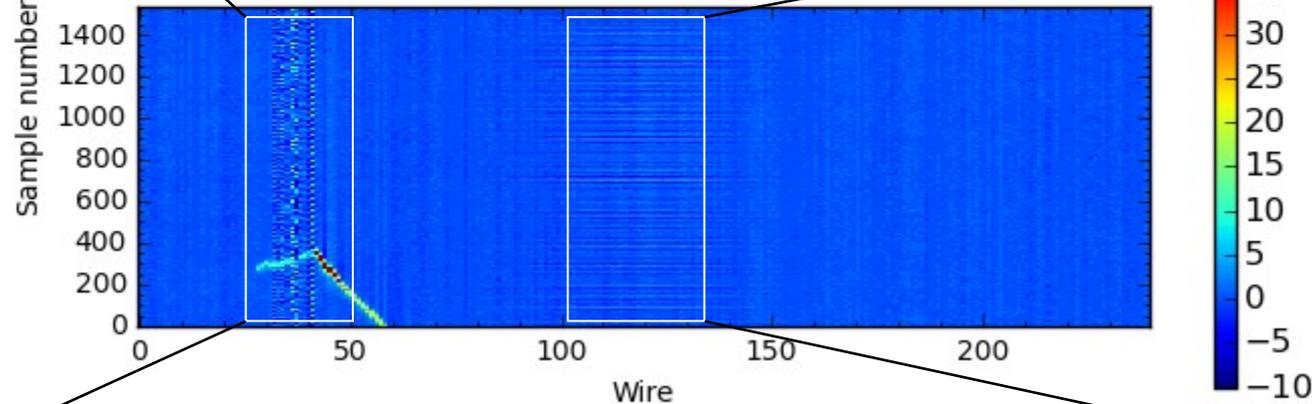
LArIAT TPC readout
Run: 5385; Spill: 4; Event: 23; Time stamp: 2015-05-04 18:27:40

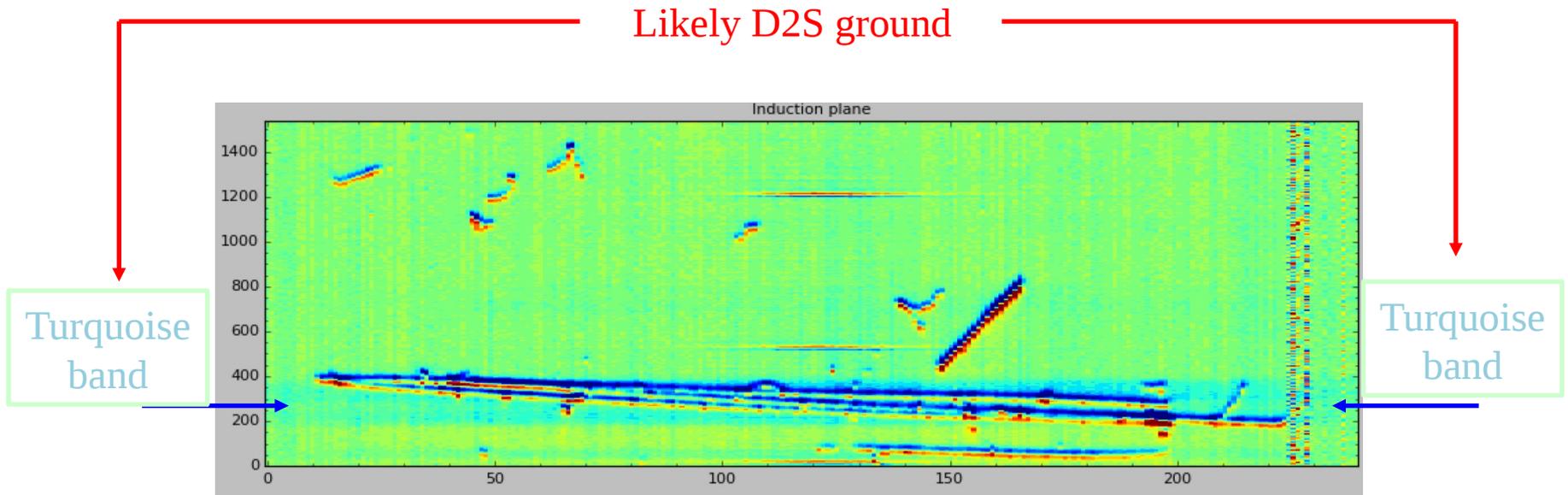
Induction plane



Better shielding needed

Collection plane





The Turquoise band seems to correspond to a crosstalk (ground bounce) in the D2S – to – CAEN connection.

We can stiffen the ground between D2S and CAEN with a modification of the D2S

Labor estimate: about one full day to extract D2S cards, solder, re-install.