Dec. 2015 Testing Results
LArIAT Analog Electronics

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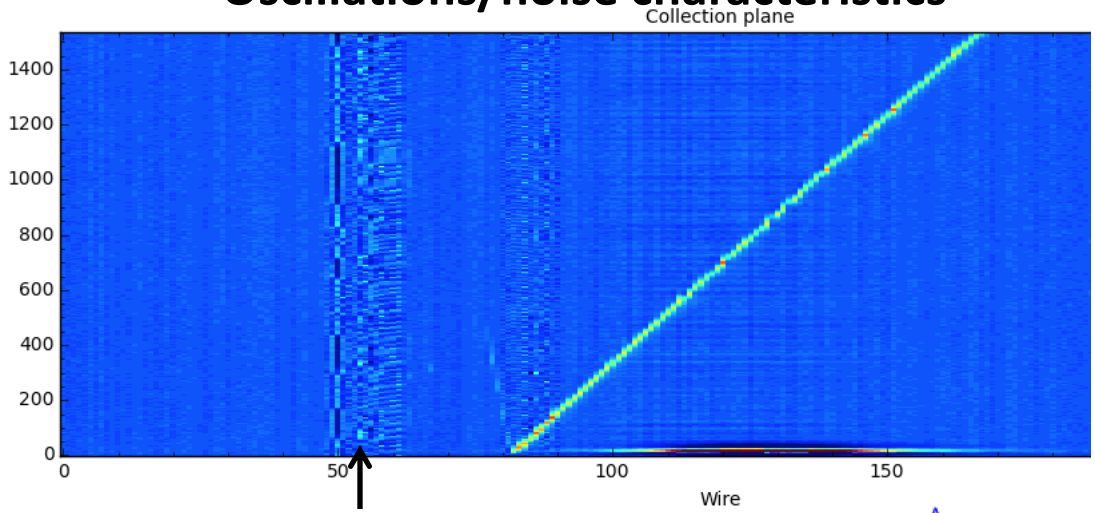
With help from Jason and Bill (others?)

New cable tray installed (Thanks!)

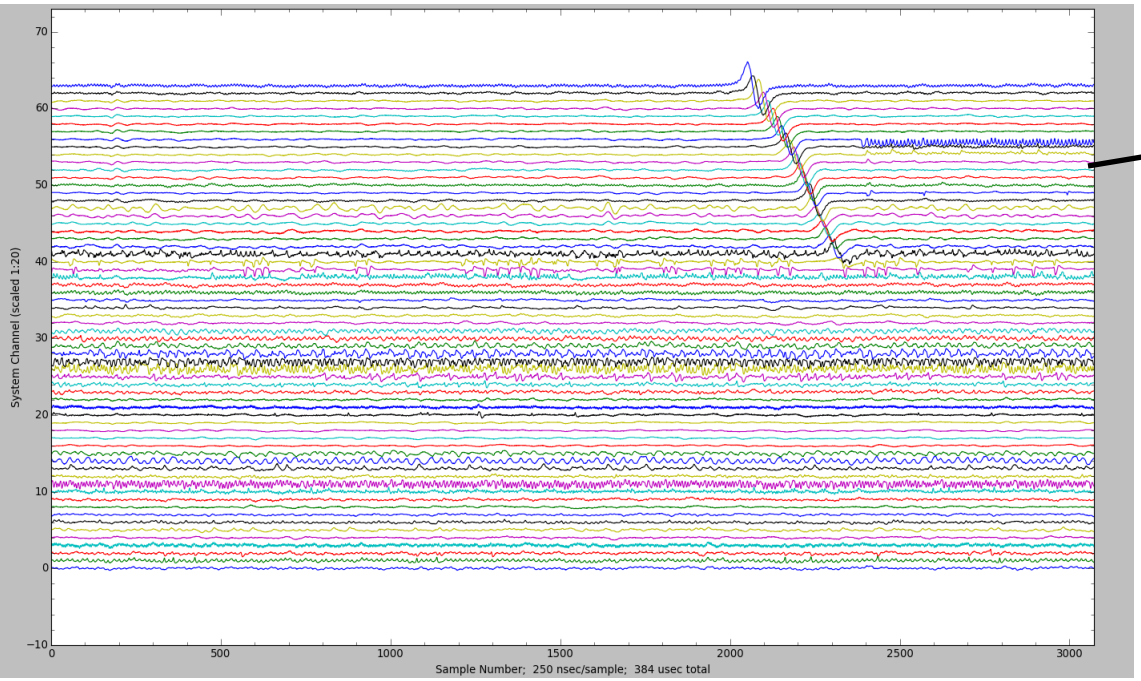
System checkout: all 480 channels are connected and pass signals

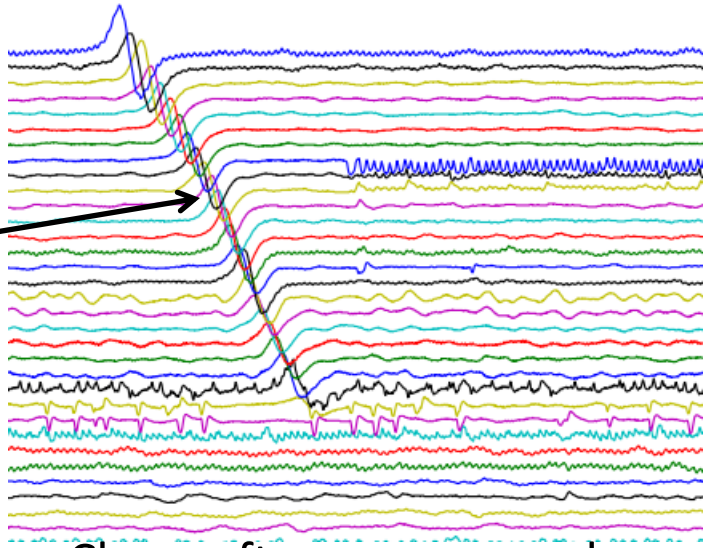
This allows us to explore noise and digital corruption issues

Oscillations/noise characteristics



Strange HF Oscillations





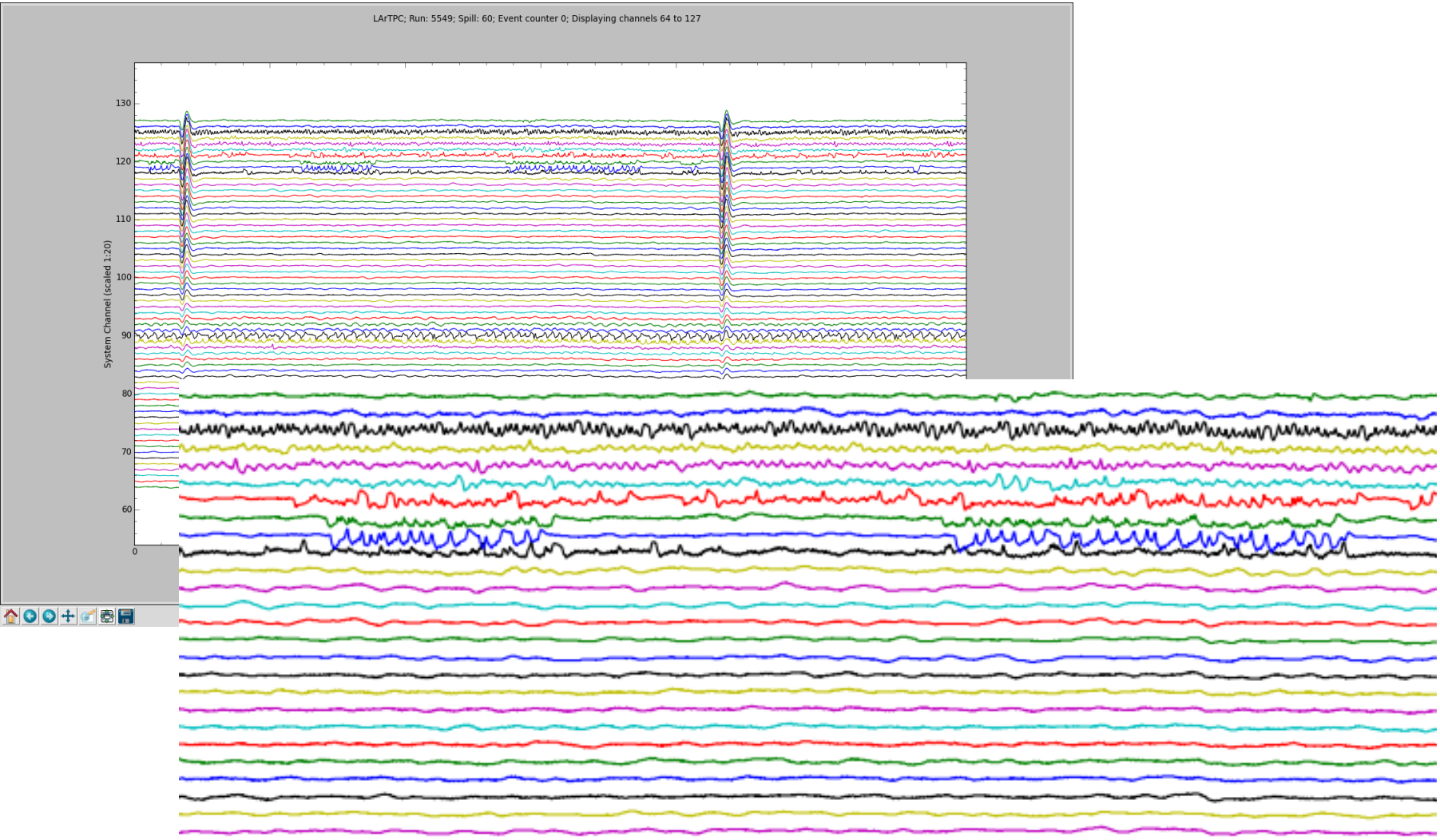
Clears after a power cycle

Idle system: <u>hours of quiet</u>

Slowly returns over 10's of spills

Can be filtered out

Oscillations observed to come and go on some channels



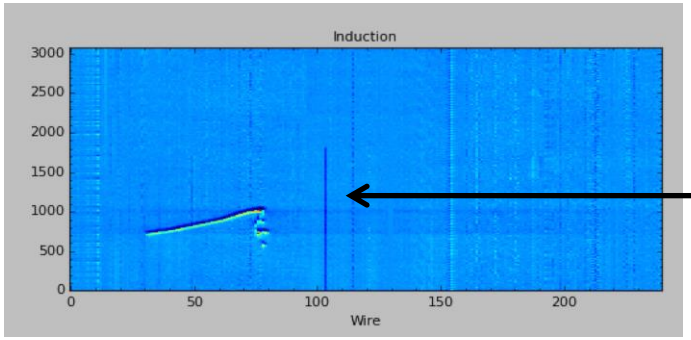
Baseline shifts/oscillations

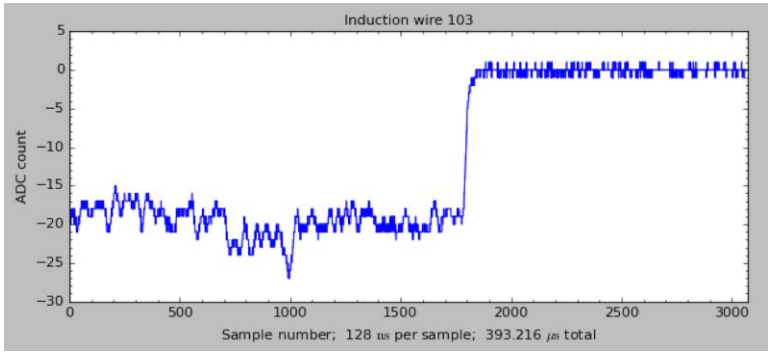
AC coupling between ASICs and WRD implies <u>baseline shift</u> is outside cryostat

<u>Oscillations</u>: could originate anywhere in the system

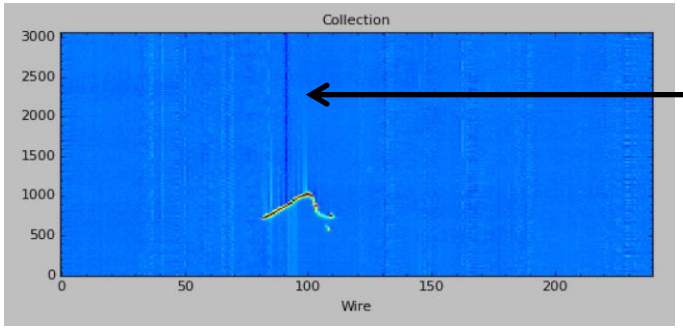
- Run 6308, Spill 2, Event 23

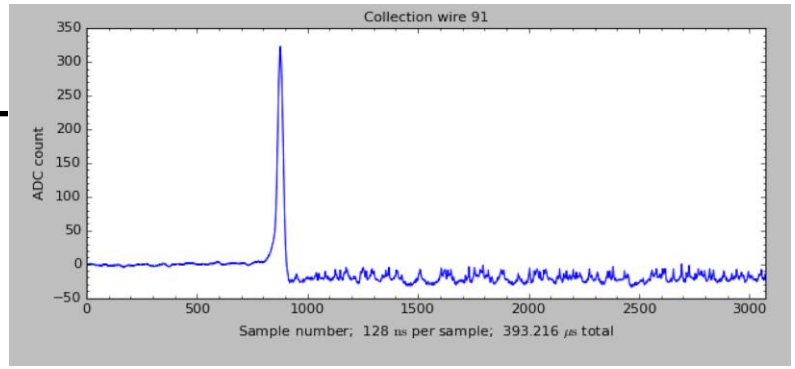
Baseline shifts from -20 to zero +/- one count



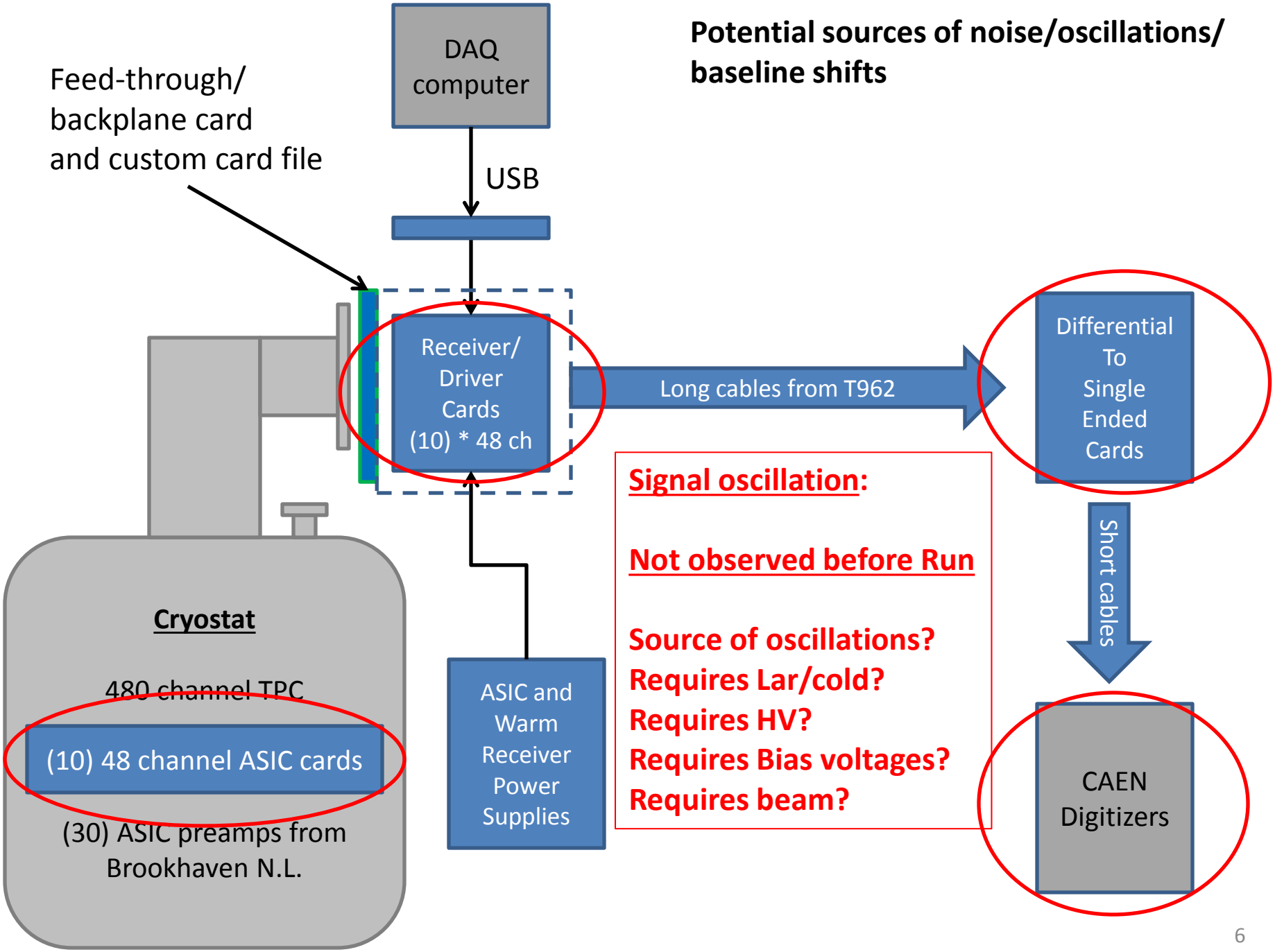


Baseline shifts from 0 to -20 with oscillations





Potential sources of noise/oscillations/ baseline shifts



Signal oscillation:

Not observed before Run

Source of oscillations?
Requires Lar/cold?
Requires HV?
Requires Bias voltages?
Requires beam?

December 1-2 visit to LArIAT

"Stop sign" cover over cryostat allows testing with TPC voltages on (reduced drift voltage).
(Thanks to all those involved with construction and paperwork efforts!)

Initially we could not replicate oscillations or baseline shifts. Hours of operation with test pulses.

Finally found a way to reliably trigger oscillations:
All ASICs set to highest gain/200 mV, then shift to lowest gain/900 mV.
→Other combinations work, weaker ASIC transitions are less likely to trigger oscillations.
→Oscillations, once started, propagate through the system until some steady-state.
→Baseline shifts correlate with noise. I have no explanation for these shifts. Some amplifier characteristic?

Model: This ASIC parameter change yields a sharp transition in the ASIC outputs, with more high-frequency components than in normal TPC or test signals.
→ This gives us enough high-frequency components to trigger oscillations.

Test:
In oscillating state: power off ASICs. Result: oscillations continue, but patterns change.
Power ASICs on again: original patterns ~restored.
Power cycle D2S: oscillations persist.

Conclusion:
(1) ASICs are not required for oscillations.
(2) ASIC output stages are involved in the oscillations (cryo cabling is part of resonant system).
(3) WRD cards appear to be the source of oscillations and baseline shifts.

Oscillation patterns: these can change with changes to system

CAEN	Channels 00-07	08-15	16-23	24-31	32-39	40-47	48-55	56-63
0	-	-	-	-	-	-	X	X
1	-	-	X	X	-	-	-	-
2	-	-	X	X	-	-	X	X
3	X	X	-	-	-	-	X	X
4	-	-	-	-	-	-	X	X
5	X	X	-	-	-	-	-	-
6	-	-	-	-	-	-	-	-
7	-	-	-	-	-	-	-	-

CAEN	Channels 00-07	08-15	16-23	24-31	32-39	40-47	48-55	56-63
0	-	-	-	-	-	-	X	X
1	-	-	X	X	-	-	-	-
2	-	-	-	-	-	-	-	-
3	X	X	-	-	-	-	X	X
4	-	-	-	-	-	-	X	X
5	X	X	-	-	-	-	-	-
6	-	-	-	-	-	-	-	-
7	X	X	-	-	-	-	-	-

X = noisy group of channels.

In Red: channels corresponding WRD48 card #4

Replace WRD48 # 4 with an unused spare card.

This caused distant changes in the patterns of oscillations.

This shows that the oscillations are a system-wide problem.

→ **cables, cards, and feed-through are all involved in the oscillation patterns.**

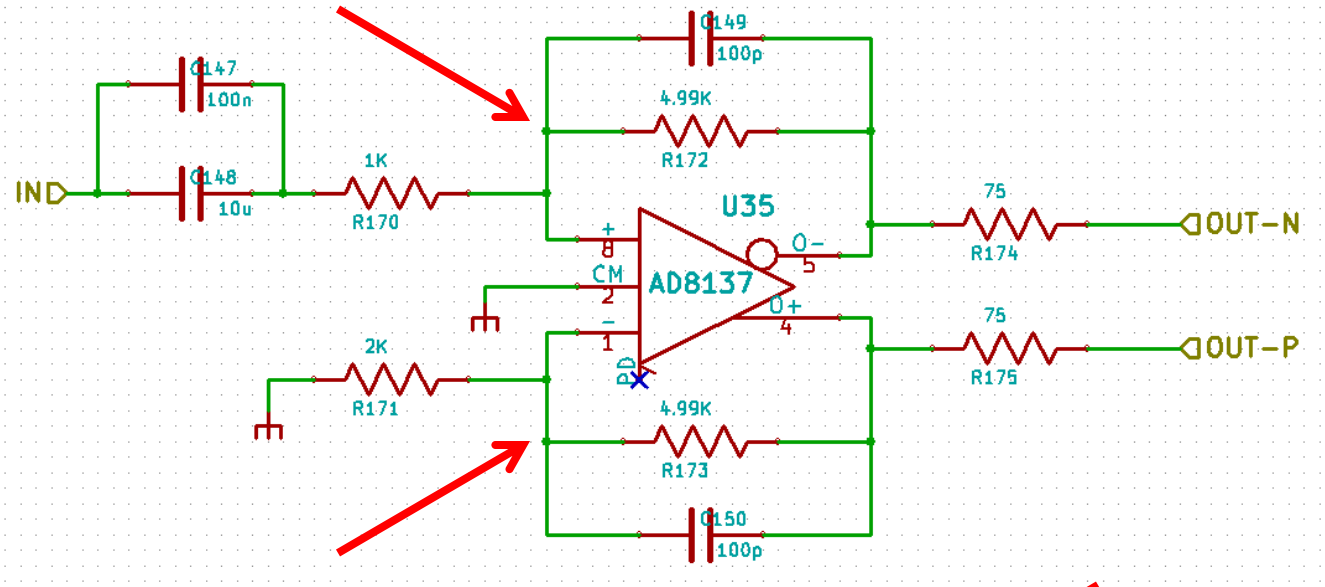
Need a real-time tool for debugging. (WaveDump has limited scope, real DAQ not appropriate).
Can we get a 48 x 10 character-matrix output from a hack of the CAEN WaveDump program?
Can WaveDump read from all CAENs at one time? (Bill? Johnny? Dean?)

Next steps:

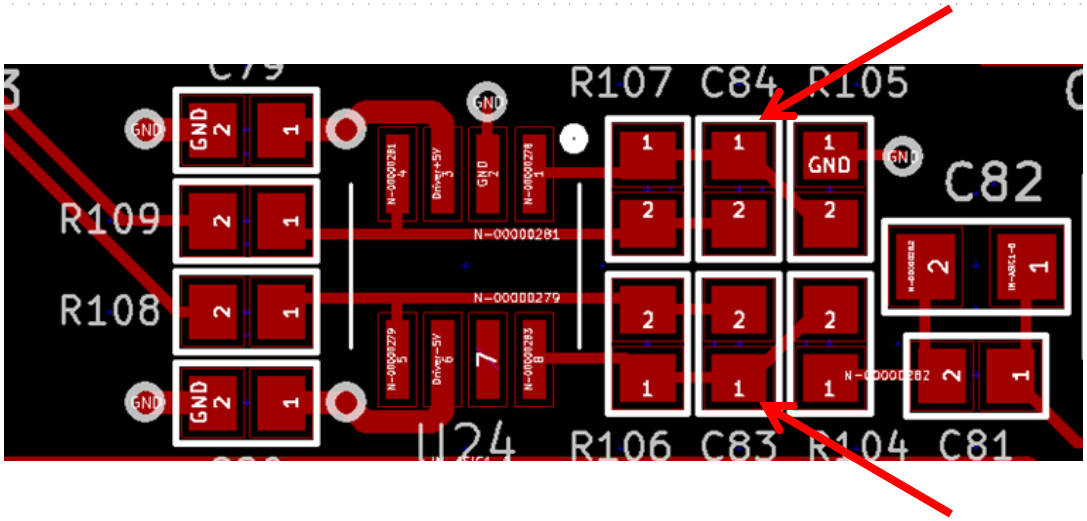
Try to reproduce the oscillations in the lab at MSU (48 channel test system).

Try to understand the source of the oscillations. Parasitic coupling at differential drivers?

Work on methods to keep us out of the oscillating state.



OUT



IN

Conclusions:

The LArIAT readout does not seem to go into oscillations without some trigger (HF noise?)

The WRD cards are the source of the oscillations (not the ASICs in the TPC)

So the cryostat can be closed? (Pending: cable mapping test, bias voltage tests?)

Current work:

Trying to reproduce the oscillations in the MSU test stand. (coming days).

Potential solutions to the noise problem:

Add shielding to the WRD-48 cards. Try to reduce parasitic couplings.
Various approaches. (Much easier if I can reproduce the noise in the lab.)

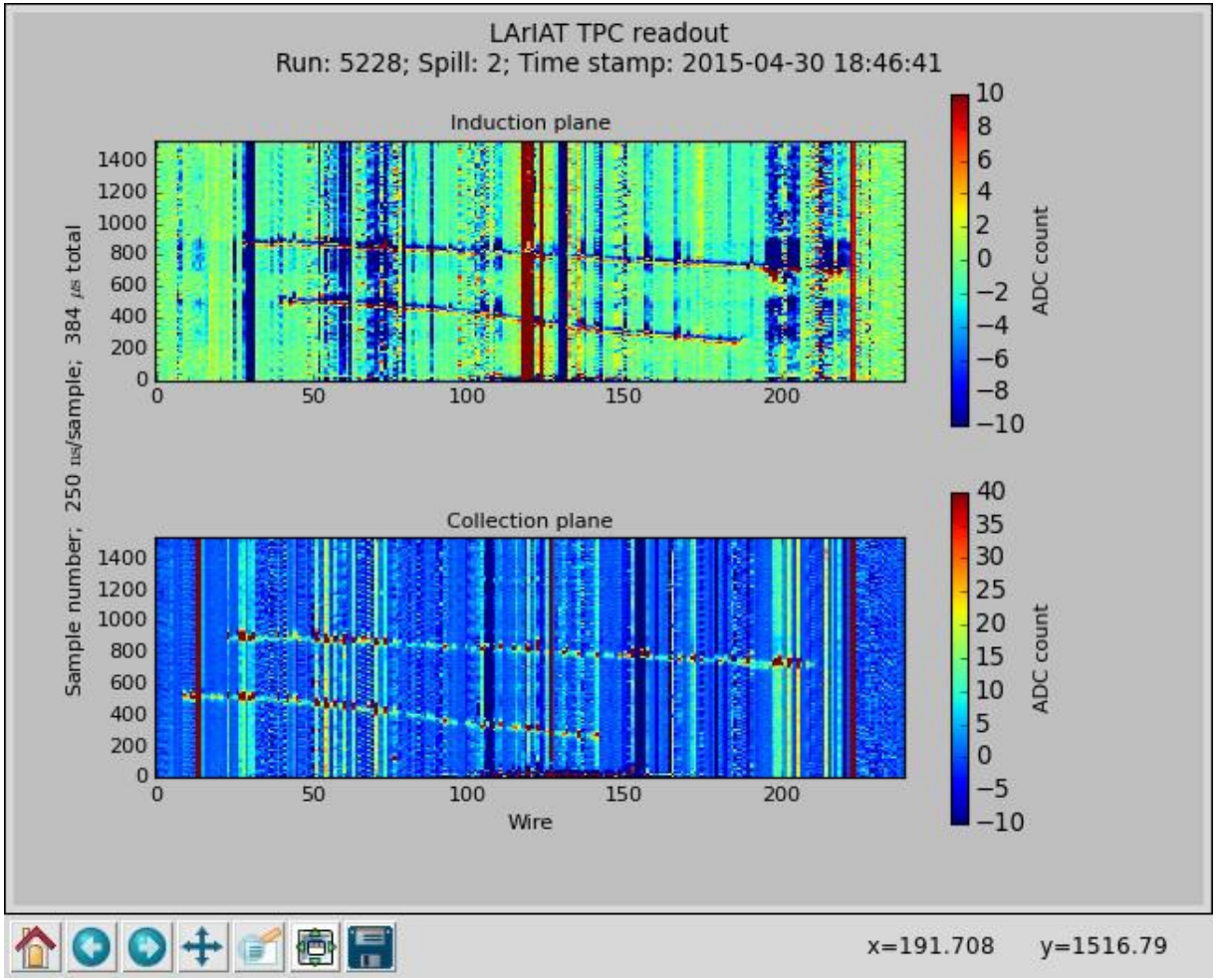
Remote power down of the WRD-48 drivers to escape the oscillating state.
(Could switch the driver power, or use amplifier shutdown pin (would require re-work of cards)
Requires real-time DQM (in between spills?)

Reduce external noise inputs, both inside and outside cryostat.
ASIC parameter corruption: a sign that there are occasionally large noise spikes in the area?

That’s all for now.

Early Run ASIC Parameter corruption

Some gain changes on groups of a few channels (not 16)



Power cycle removes noise temporarily

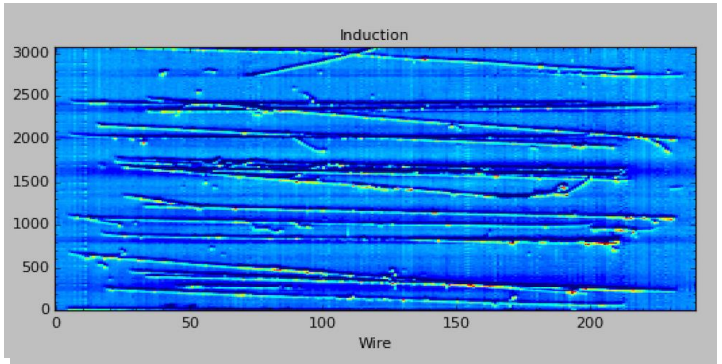
ASIC download restores parameters temporarily

Changed serial line impedance & added Serial line readback

BUT Channels dead/alive mid spill !

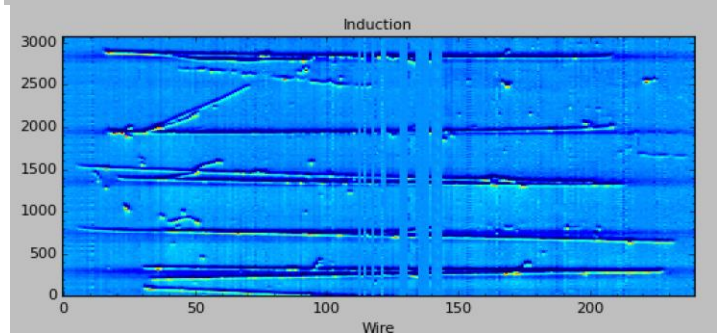
- Run 6308, Spill 2

Event 8, Spill Time 5.05 s

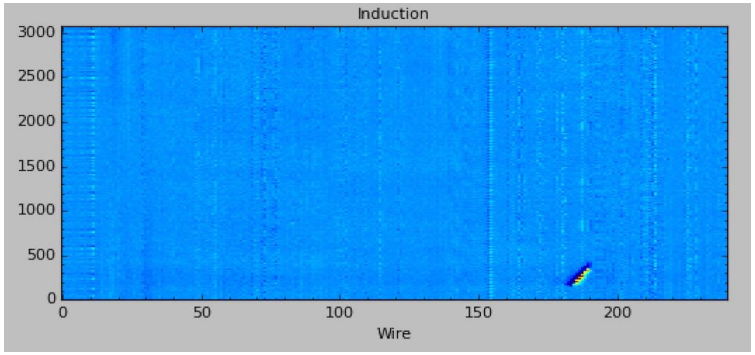


30 msec later

Event 9, Spill Time 5.08 s



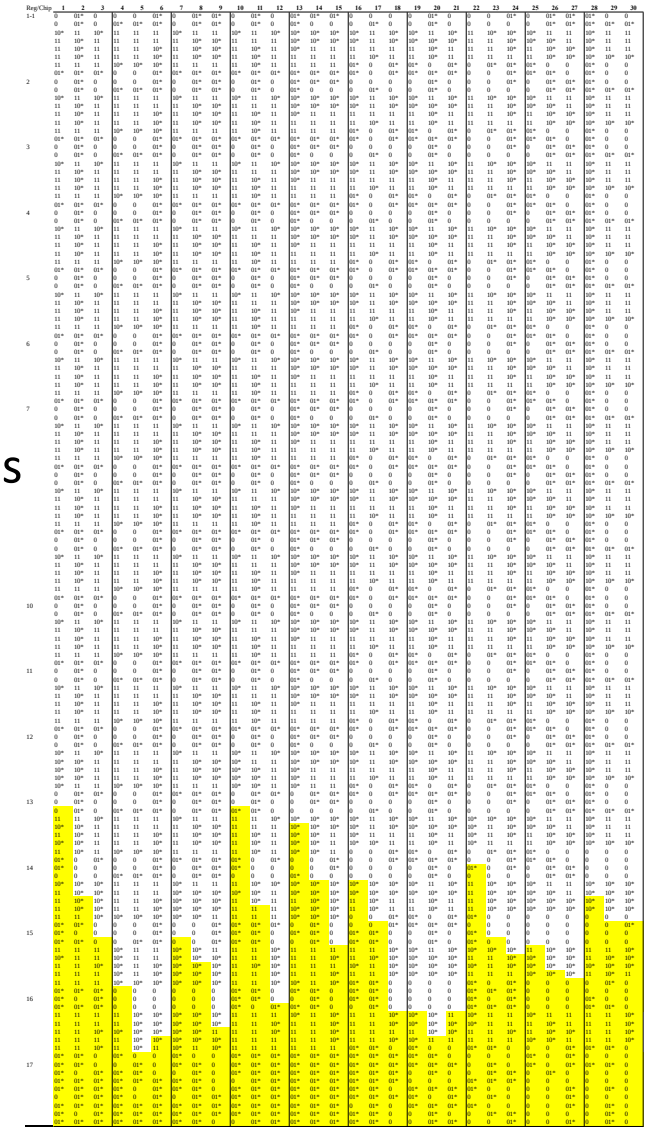
Event 10, Spill Time 6.05 s



Linda Bagby (uBoone) suggests this is ASIC saturation

After changes to ASIC serial line impedance corruption may have changed

Downloading of ASIC after each spill good for data but confuses the issue.



136 bits /ASIC

Correct bits are shifted up

A few times/day
Correct bits are shifted up

To minimize the amount of data affected
correct bits downloaded after each spill

Intentionally generated noise sources
DON'T cause the corruption

0 or 1 bits inserted

30 ASICs