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## 1. System overview

The LArIAT TPC front-end electronics comprises a 480-channel analog signal path from the liquid argon time projection chamber (TPC) to the signal digitizers. The front-end system also includes a digital control system for the TPC-mounted electronics, a power supply and distribution system, and mechanical structures for support of the different circuit boards. A block diagram of the overall system is shown in Figure 1.

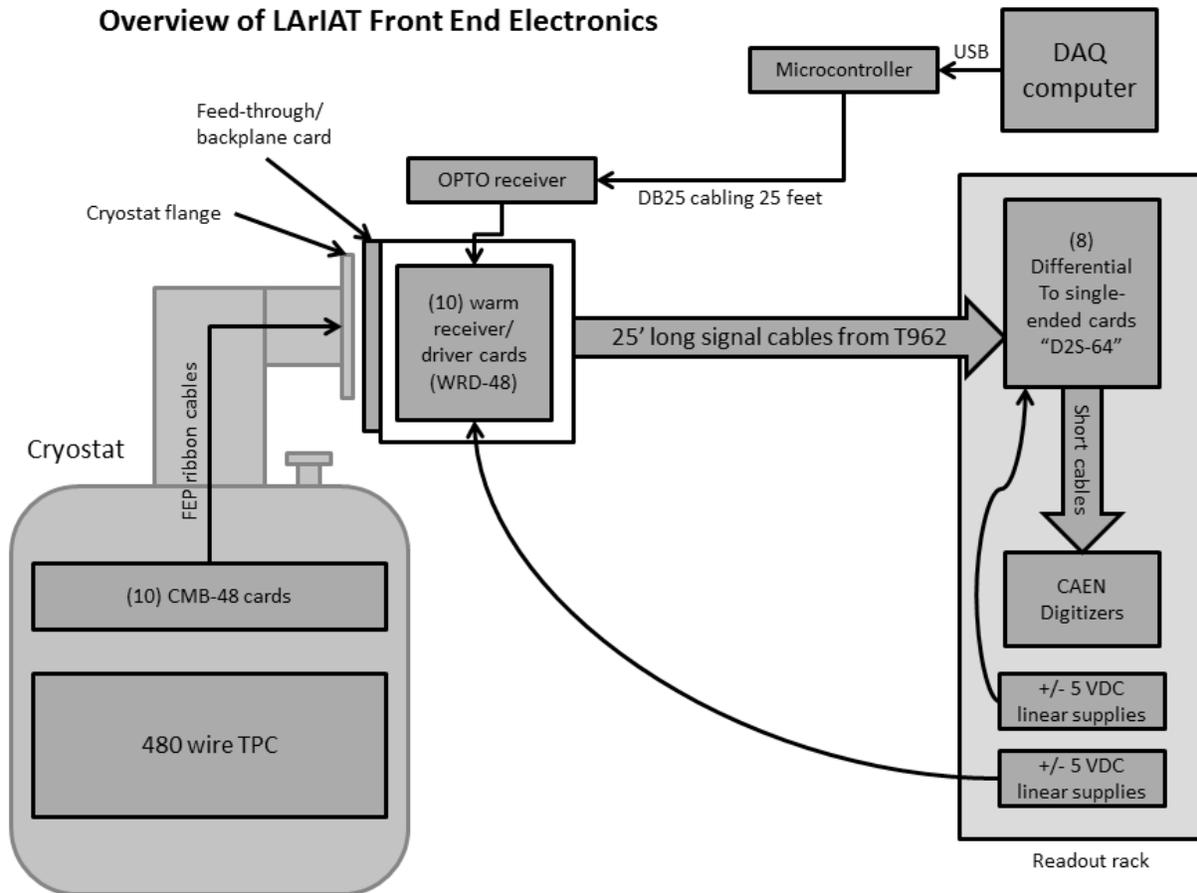


Figure 1.

This document describes the overall LArIAT TPC front-end system at the level of the individual subsystems. This format is chosen because the different subsystems are distributed across different physical sections (circuit boards) of the overall system. It is easiest to understand the overall system by studying one subsystem at a time. The engineering details at the circuit board level are presented in the appendix of this document.

## 2. Analog signal path

In a liquid argon TPC, the analog signals originate as ionization of the liquid argon along particle tracks inside the TPC volume. The electrons liberated by ionization drift in an electric field toward planes of detection wires. In LArIAT, the drifted electrons encounter three successive planes of wires, termed the shield plane, the induction plane, and the collection plane. The planes are electrically biased such that the shield plane and the induction plane are transparent to the passage of electrons, while the collection plane absorbs the electrons. In LArIAT, the wires of the induction plane and the collection plane are capacitively coupled to amplifiers for readout. The signals from the induction plane are bipolar, while the signals from the collection plane are unipolar.

With the LArIAT TPC wire spacing (4 mm) and the expected energy deposition of a passing MIP, it is expected that under ideal conditions a charge of about 3.5 fC will arrive at an individual TPC readout wire.

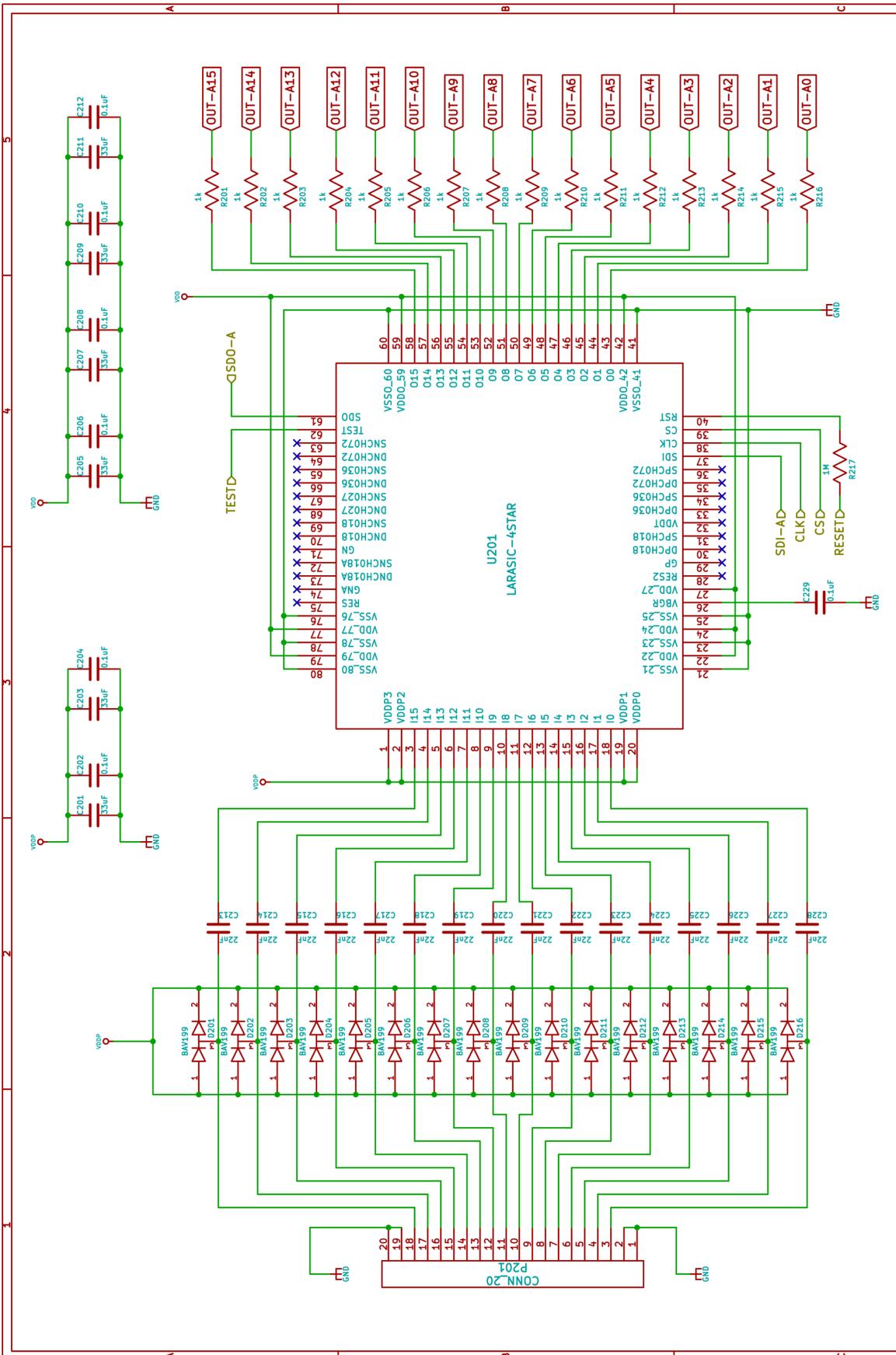
The electrical signals on the TPC readout wires are a direct readout of the ionization of the liquid argon. These signals can be quite small: one of the major challenges in TPC electronics is achieving a good SNR (signal-to-noise ratio) for these weak signals. The drive for improving the SNR has spurred the development of cold amplifiers that are mounted directly to the TPC inside the liquid argon cryostat. This arrangement places the amplifiers as close as possible to the signals and also allows the leveraging of cryogenic conditions in the electronics design. The LArIAT TPC (Run 1) is instrumented with cold amplifiers developed by Brookhaven National Lab. The BNL amplifiers are built as custom application-specific integrated circuits (ASICs). The BNL ASICs are designated as LArASIC, and in LArIAT Run 1 the TPC has been instrumented with LArASIC version 4-star. The LArASIC 4-star datasheet should be included in the same location as this document; alternatively, it is available from BNL.

The LArASICs are mixed signal devices, where the analog amplifier characteristics are controlled by digitally-set parameters. The maximum gain setting of the LArASIC is 25 mV / fC. At this gain we expect that a 3.5 fC charge deposition on a readout wire will generate an output with about 90 mV amplitude. At the other end of the readout chain, the digitizers (CAEN model V1740) have a 12 bit resolution and a maximum input range of 2 VDC, yielding about 0.5 mV LSB. Given this combination of expected signal amplitude and digitizer input range, the analog signal path from LArASIC to the digitizers has been designed to provide unity gain. With the unity gain analog path, we expect that a passing MIP will generate a digital signal with amplitude of about 180 ADC counts.

In the LArIAT experimental hall the TPC and the readout rack containing the digitizers are separated by about 25 feet. With this distance between the signal source and the signal readout there is a difficulty in transmitting single-ended signals, since the ground reference at the two locations will differ. Additionally, with single-ended signals, any noise pickup along the path will be mixed with the signal. To overcome these difficulties the single-ended analog signals from the ASICs are transmitted from the cryostat to the distant readout rack as differential analog. At the receiving end of the differential path the differential-mode analog signal is amplified and the common-mode signal is rejected. This arrangement provides a solution to both the problem of differing grounds and the problem of common-mode noise pickup.

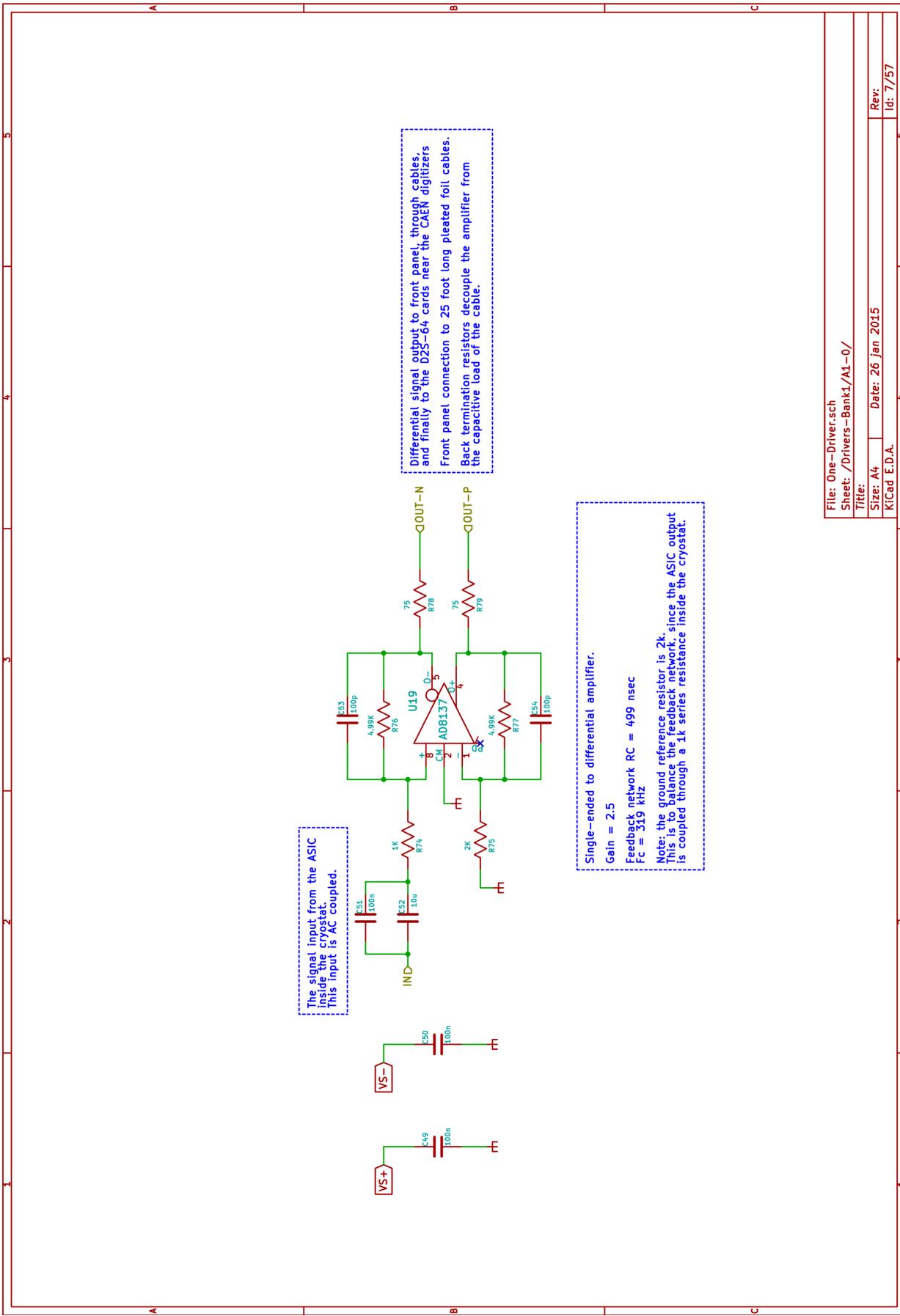
Given the design requirements of overall unity-gain and differential analog signal transmission, a signal path was developed to carry the analog information from the ASICs on the TPC to the CAEN digitizers. The resulting signal path is distributed across a series of four types of interconnected cards.

The first type of card in the system is a 48-channel cold motherboard (CMB-48) that mounts directly to the TPC and houses three 16-channel LArASICs per card. The analog signal path on this card is shown in Figure 2. The next card in the signal path is a single cryostat feed through card (FT) that carries the 480 signal lines (along with power and control lines) across the cryostat boundary. A set of warm receiver and driver (WRD-48) cards plug directly into the cryostat feed through and amplify the single-ended TPC signals as differential analog. The analog signal section of the WRD-48 is shown in Figure 3. The differential analog signals are driven through 25 foot long high quality pleated foil cables that were still on hand from the ArgoNeuT experiment. At the far end of the pleated foil cables a set of differential-to-single-ended (D2S-64) cards convert the differential signals into single-ended signals with enough drive capability to allow direct input into an array of CAEN V1740 digitizers. The signal path on the D2S-64 is shown in Figure 4. The engineering details for the different cards are presented in the appendix.



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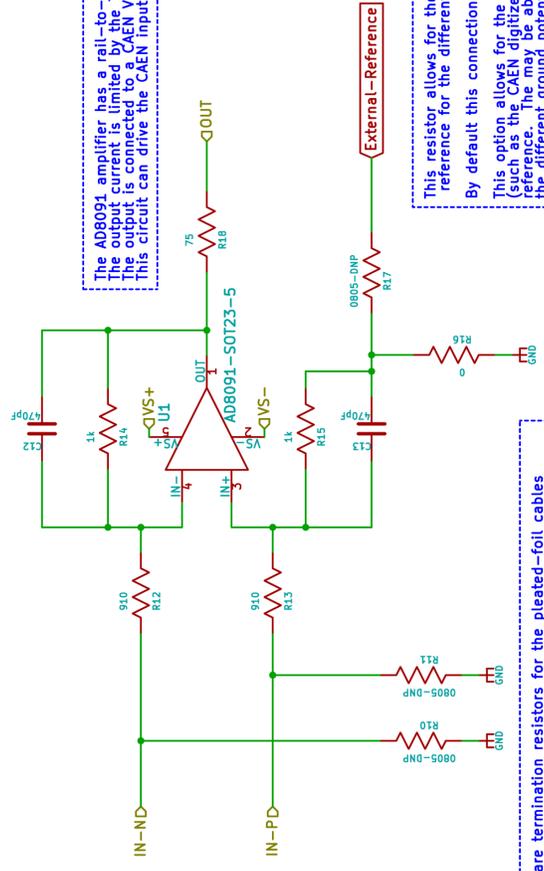
The signal input from the ASIC inside the cryostat. This input is AC coupled.

Differential signal output to front panel, through cables, and finally to the D2S-64 cards near the CAEN digitizers. Back termination resistors decouple the amplifier from the capacitive load of the cable.

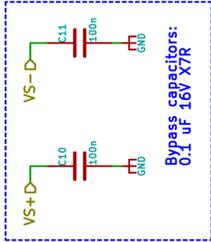
Single-ended to differential amplifier.  
 Gain = 2.5  
 Feedback network RC = 499 nsec  
 FC = 319 kHz  
 Note: the ground reference resistor is 2k. This is to balance the feedback network, since the ASIC output is coupled through a 1k series resistance inside the cryostat.

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Differential to single-ended amplifier.  
 Gain (including source impedance of 75 Ohm) is about 1.02  
 The RC in the feedback loop is 0.47 microseconds.  
 This will roll off the gain for signals above the frequencies of interest.



The AD8091 amplifier has a rail-to-rail output section. The output current is limited by the 75 ohm output coupling resistor. The output is connected to a CAEN V1740 digitizer with 50 ohm input termination. This circuit can drive the CAEN input to (+/-5V)/(125 ohms) = +/- 2V.



These are termination resistors for the plated-foil cables. We are dealing with slow signals (150 kHz), so the termination resistors are not necessary.  
 These circuit elements are specified so that the circuit board copper layout includes the possibility of adding termination resistors as an optional feature.

This resistor allows for the optional connection of an external reference for the differential to single-ended amplifier.  
 By default this connection will not be enabled.  
 This option allows for the ground of an external device (such as the CAEN digitizer) to be used as the output reference. It may be able to reduce signal noise caused by the different ground potentials of the D2S and the input of the CAEN digitizer.

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### 3. ASIC digital controls

The LArASIC chips are mixed-mode ASICs, where the analog characteristics of the amplifiers are controlled by digital registers. This section describes the layout of the digital controls, the monitoring of the digital control lines, the generation of the bit stream that configures the ASICs, and the connections between the ASIC controls and external computing equipment.

#### 3.1. Layout of the Digital Controls

The digital portion of each ASIC exists as a shift register with a length of 136 bits. This shift register contains 8 configuration bits per amplifier channel plus an additional 8 bits to set global parameters for the ASIC. The definition of the ASIC control bits is detailed in the LArASIC 4-star data sheet.

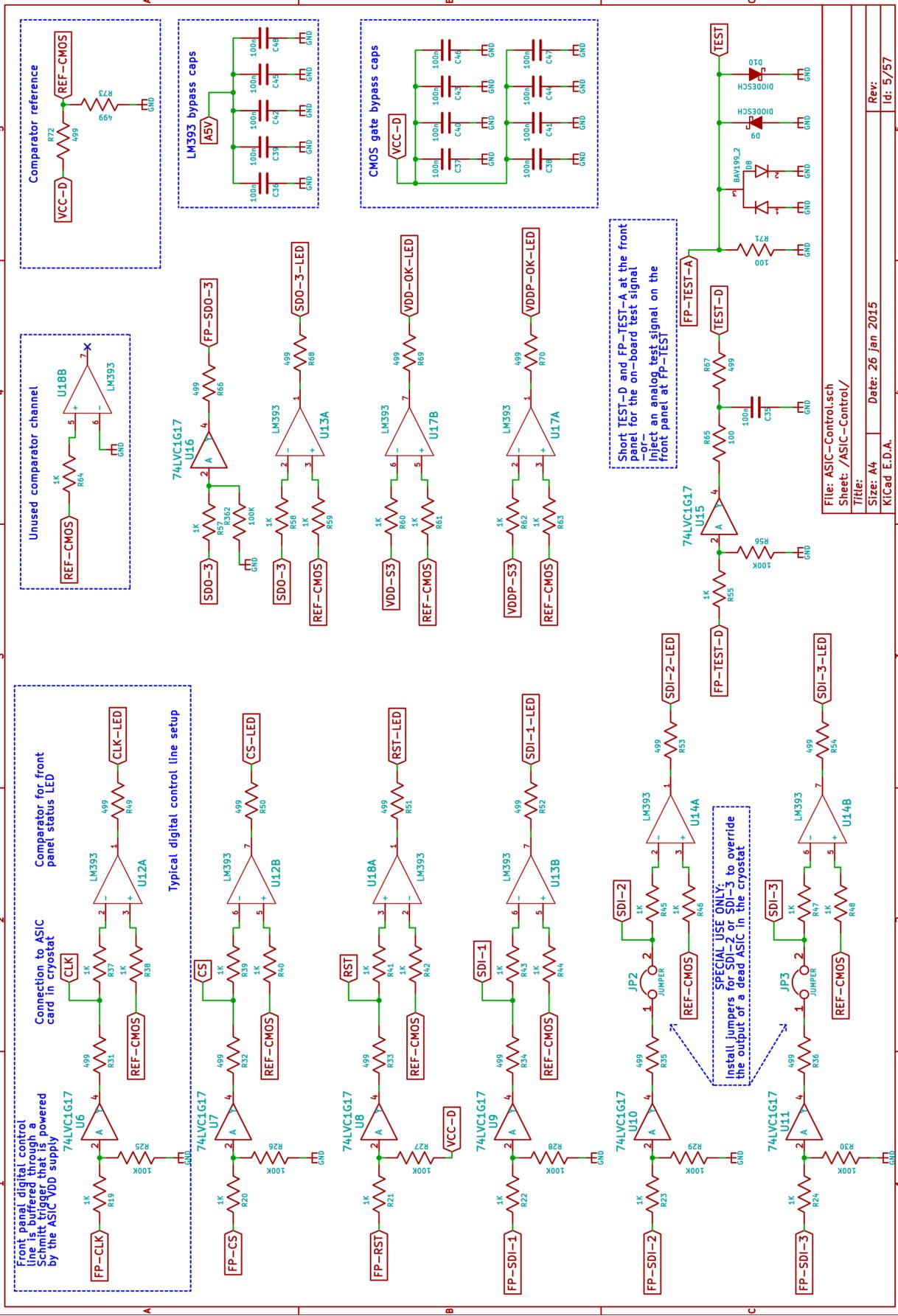
The LArASIC shift register is programmed by a combination of clock (CLK), serial data in (SDI), reset (RST) and chip-select (CS) lines. The serial data out (SDO) from the far end of the ASIC shift register is also available. This configuration allows for an arbitrary number of LArASICs to be daisy-chained by connecting the SDO of one ASIC to the SDI of the next ASIC and by distributing the CLK, CS, and RST in parallel across all ASICs. In this way the 30 ASICs comprising the entire 480-channel LArIAT TPC readout can be controlled with only four external digital inputs.

However, there is a serious risk in embedding a serial daisy chain inside a cryostat where access is limited or even impossible for long periods of time. If a single link along the chain fails then there is no possibility of propagating signals beyond the break in the chain. An even more serious possibility is a shorted input gate that holds a distributed control line against one of the power supply rails, thus disrupting the entire system.

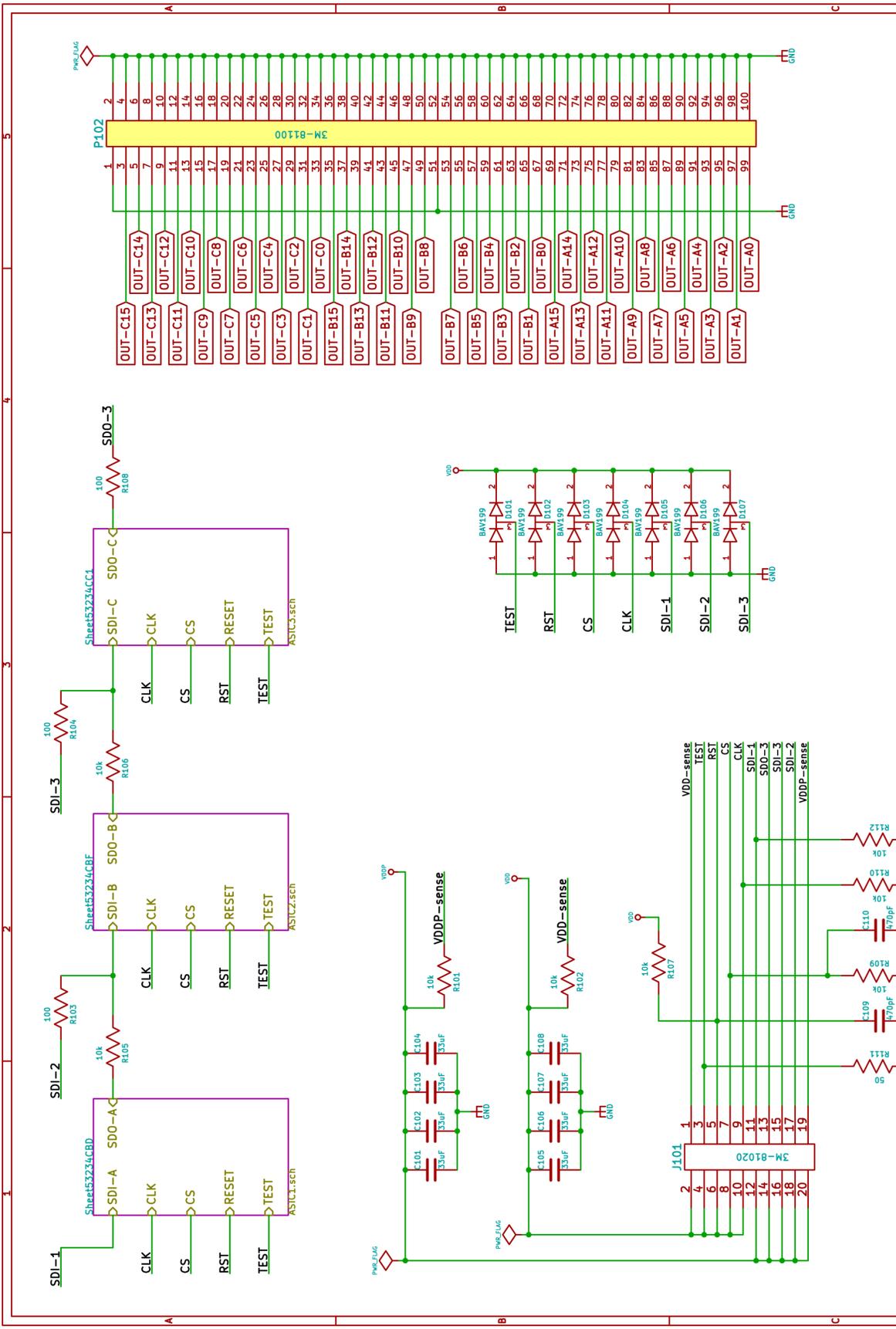
The LArIAT digital controls system was designed avoid these potential single point failures by providing external user access to the digital interconnections. The digital control lines for each 48-channel (3 ASIC) cold motherboard (CMB-48) are presented at the front panel of the corresponding WRD-48 card on top of the cryostat. This arrangement allows for the daisy chain from one CMB-48 to the next to be made with a jumper between the front panels of the corresponding WRD-48 cards (SDI to SDO jumpers). Additionally, in the event of a shorted digital input on an ASIC, only one CMB-48 card will be affected. These connections are easily accessible and do not require any intervention inside the cryostat.

The front panel access of SDI to SDO connections from one CMB-48 to the next makes it possible to bypass a faulty CMB-48. However, a faulty CMB-48 card would still result in the loss of 48 channels (10%) of the LArIAT TPC readout. To insulate against this possibility the two SDI-SDO connections between the three ASICs on each CMB-48 card are monitored and can optionally be driven from the WRD-48 cards. To achieve this functionality, each of the two on-card SDI-SDO connections on a CMB-48 card are connected through 10k ohms of resistance and the SDI-side of the 10k ohm coupling resistance is connected to the WRD-48 card. This allows any SDI-SDO connection in the system to be monitored from the outside of the cryostat. Additionally, in the event of an ASIC failure where the shift register is broken, the SDO output of the failed chip can be overridden by driving the interconnection from the WRD-48 card.

The digital control and monitoring section of a WRD-48 card is shown in Figure 5. The digital controls section of the CMB-48 card is shown in Figure 6.



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Rev: 2.0	Id: 1/4



### **3.2. Monitoring of the Digital Control Lines**

During operation it is important to be able to quickly diagnose any problems with the digital controls system. Front panel indicators on each WRD-48 card allow the digital control lines leading to each CMB-48 to be monitored. The lines are monitored by an independent digital subsystem of voltage comparators driving front panel LEDs. This configuration allows the actual digital state of the control lines to be monitored, which can be quite helpful for finding shorted or open control lines. Each WRD-48 card shows the digital status of all digital control lines leading to the corresponding CMB-48 card. Additional LEDs on the front panel show the status of the WRD-48 power inputs. The array of comparators that monitor the digital lines were shown in Figure 5. The layout of the WRD-48 front panel LED indicators are shown in the appendix.

### **3.3. Generation of the ASIC Control Bit Stream**

The generation of the bit stream for programming the ASIC parameters is a relatively trivial task which could be performed at many different levels in the LArIAT system. During stable running with particle beams is it best to have the digital controls originate inside the DAQ architecture. However, for commissioning and diagnostics, it is quite useful to have full control of the digital system from a standalone or portable computer (such as a laptop). To suit both control options a small microcontroller with a USB interface was used to generate the bit stream that programs the ASICs. The USB port on the microcontroller allows for easy connection either to the DAQ computers or to a standalone computer. The microcontroller runs a simple command line interface with human-readable commands allowing easy control of the system. The microcontroller chosen for the task is the inexpensive Teensy 2.0 from PJRC.com. The choice of this microcontroller was made based on low cost, ease of use, a wide user base, and an open-source development platform. The C programs that runs on the microcontroller should be included with this documentation.

### **3.4. Digital Connections to the Cold Electronics**

The electrical connection of the microcontroller (or any other hardware) to the TPC electronics presents a risk of introducing electrical noise or ground loops into the overall system. Additionally, a direct electrical connection creates the risk of damaging the electronics inside the cryostat through some external electrical mishap. In order to guard against these possibilities the digital control lines are isolated through optocouplers to provide galvanic isolation. The optocouplers are located at the WRD-48 card file on top of the cryostat, and they are driven from the Teensy microcontroller which is located near the DAQ computers. The Teensy drives the optocouplers through a commercially available DB-25 cable assembly. With this configuration there is no direct electrical connection between the TPC control electronics and external computers.

When performing diagnostics or hunting electrical noise it can be very helpful to be able to disconnect portions of a distributed system during operation. The use of the optocouplers to isolate the ASIC digital control signals allows the DB-25 control cable to be safely disconnected or reconnected while the overall system is powered and running. The LArIAT controls are configured to place all optocouplers in the off (unpowered) state when the control lines are idle. (note: to achieve this configuration, the digital state of the active-low RST line is inverted at the opto receiver box: an unpowered RST optocoupler results in the RST line held at the idle state of 1.8 volts. All other digital lines are not inverted). This configuration means that the DB25 control cable can be disconnected without disturbing the logic state of any of the idle control lines.

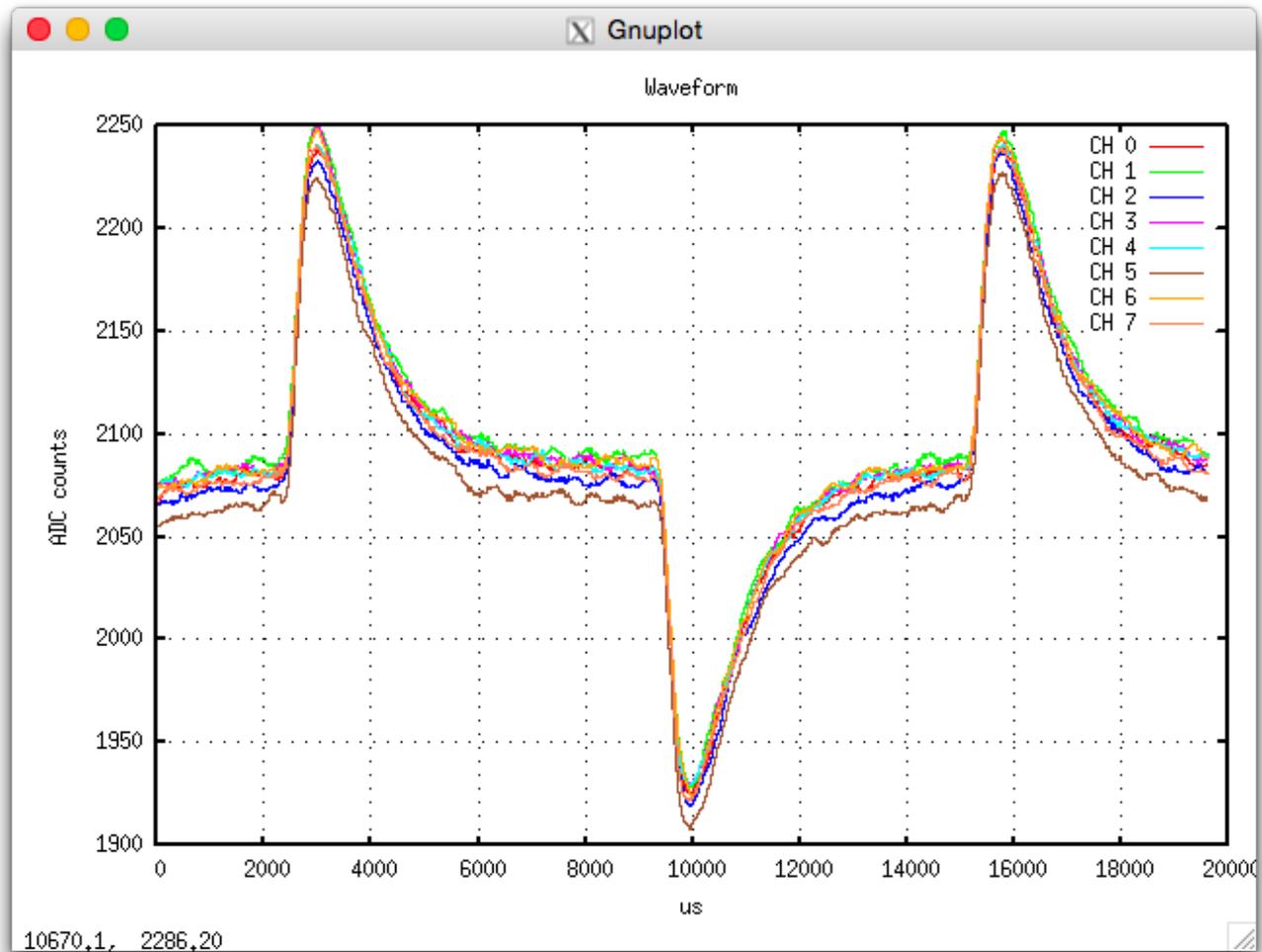
#### **4. ASIC test signal inputs**

In a multichannel readout system it is quite useful to have a pathway to deliver a test signal into the front end of the system. Each analog channel in the LArASICs has a capacitively-coupled connection to allow such a test signal input. This test capacitance can be enabled or disabled for any combination of readout channels through the corresponding ASIC digital configuration registers.

The WRD-48 cards have a simple test pulse generator circuit built in. The circuit is simply a digital gate driving an RC circuit that rounds off the pulse edges. The design was chosen for simplicity, allowing for a characteristic signal to be delivered to the ASICs on the corresponding CMB-48 card. In the current configuration (LArIAT Run 1), the test pulsers on each WRD-48 card (10 cards in total) are driven in parallel from a single digital output on the Teensy microcontroller. This allows the test pulse circuits to be controlled from within the DAQ architecture.

A more sophisticated test signal system would utilize a dedicated external waveform generator. Ideally this external signal source would be an arbitrary waveform signal generator that could be remotely controlled and also remotely connected to any individual WRD-48 card. This option is detailed in the section on upgrade pathways.

The selection of on-board test pulser or external signal generator is made at the front panel of the WRD-48 cards. The on-board test pulser is enabled with a front panel jumper. To connect an external test input the front panel jumper is removed and the external signal source is connected to the exposed front panel header. The on-board pulser circuitry is visible in Figure 5. The front panel connections for the test pulse connections are shown in the appendix. Typical waveforms read out at the level of the CAEN digitizers are shown in Figure 7.



## 5. Power distribution

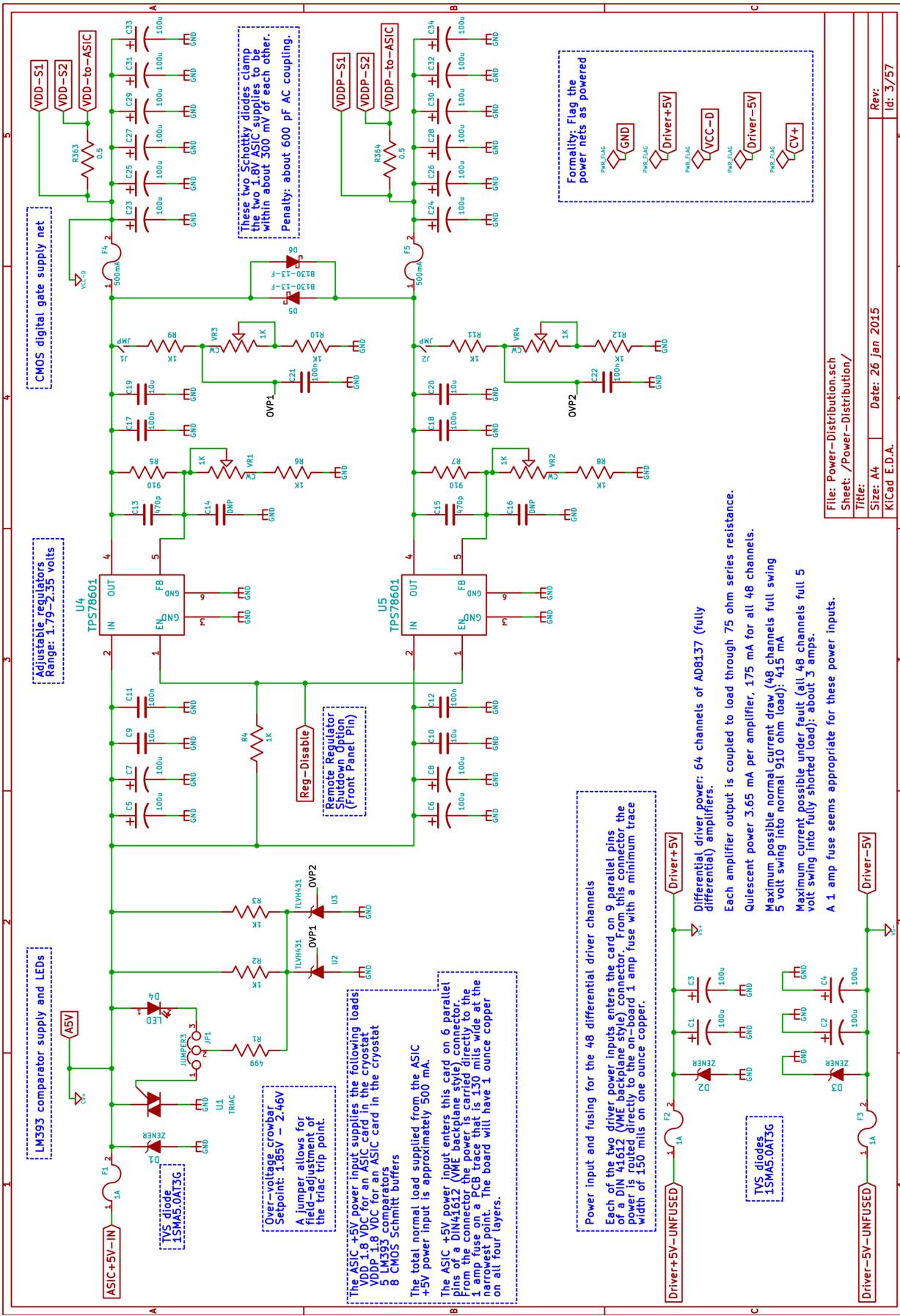
The LArASICs are specified to run at 1.8 VDC with separate power inputs to the preamp section (VDDP) and other sections (VDD) of the chip. The cleanliness of the power to the ASICs is quite important to the noise performance of the system. Additionally, at such low operating voltages it is important to carefully control the voltage, since even small voltage drops in a low voltage system can be relatively significant.

There are two general classes of voltage regulation: closed loop and open loop systems. Closed loop systems sense the voltage at the load and then make compensations at the voltage source. Closed loop systems can maintain precise voltages and compensate for drift in the system, but they are also susceptible to problems of noise and oscillations. For the ASIC power in LArIAT a trimmed open loop voltage regulator was selected.

Adjustable open-loop voltage regulators for each CMB-48 card are located on the corresponding WRD-48 card. These regulators are supplied with fused 5 VDC power which comes from standard 5 VDC linear power supplies. Linear power supplies were selected to avoid the noise that is inherent in switching power supplies. Voltage monitor lines are connected to the CMB-48 cards and are routed to

the WRD-48 front panels. This configuration allows for easy monitoring and adjustment of the voltage delivered to the CMB-48 cards. Additionally, the regulator output voltage and voltages on either side of current-sensing resistors are available on the WRD-48 front panel. The front panel connections for voltage monitoring are shown in the appendix.

The cold electronics inside the cryostat can be damaged by excessive supply voltages. To guard against overvoltage conditions, adjustable crowbar circuits are installed on the WRD-48 cards. These crowbar circuits independently monitor both the VDD and VDDP voltages. If either VDD or VDDP exceeds a defined set point then a TRIAC across the 5 VDC input will be triggered. If the TRIAC is triggered then the 5 VDC input will be held near ground until the on-board fuse is blown. The crowbar circuits have jumpers to allow for a test voltage to be injected, and also have jumpers to select an indicator LED instead of the TRIAC. This setup allows for easy adjustment and validation of crowbar circuits. The details of the voltage regulators and the crowbar circuits are shown in Figure 8.



Adjustable regulators  
Range: 1.79–2.35 volts

CMOS digital gate supply net

These two Schottky diodes clamp the two 1.8V ASIC supplies to be within about 500 mV of each other. Penalty: about 600 pF AC coupling.

Formality: Flag the power nets as powered

LM393 comparator supply and LEDs

Over-voltage crowbar  
Setpoint: 1.85V – 2.46V  
A jumper allows for field-adjustment of the triac trip point.

The ASIC +5V power input supplies the following loads:  
VDD 1.8 VDC for an ASIC card in the cryostat  
VDDP 1.8 VDC for an ASIC card in the cryostat  
8 LM393 comparators  
8 CMOS Schmitt buffers

The total normal load supplied from the ASIC +5V power input is approximately 500 mA.

The ASIC +5V power input enters this card on 6 parallel pins of a DIN41612 (VME backplane style) connector. From the connector, the power is carried directly to the board on a 1.27 mm pitch 6-pin connector. The board has a narrowest point. The board will have 1 ounce copper on all four layers.

Power input and fusing for the 48 differential driver channels  
Each of the two driver power inputs enters the card on 9 parallel pins of a DIN 41612 (VME backplane style) connector. From this connector, the power is routed directly to the on-board 1 amp fuse with a minimum trace width of 150 mils on one ounce copper.

Differential driver power: 64 channels of AD8137 (fully differential) amplifiers.  
Each amplifier output is coupled to load through 75 ohm series resistance.

Quiescent power 3.65 mA per amplifier, 175 mA for all 48 channels.  
Maximum possible normal current draw (48 channels full swing 5 volt swing into normal 920 ohm load): 415 mA

Maximum current possible under fault (all 48 channels full 5 volt swing into fully shorted load): about 3 amps.

A 1 amp fuse seems appropriate for these power inputs.

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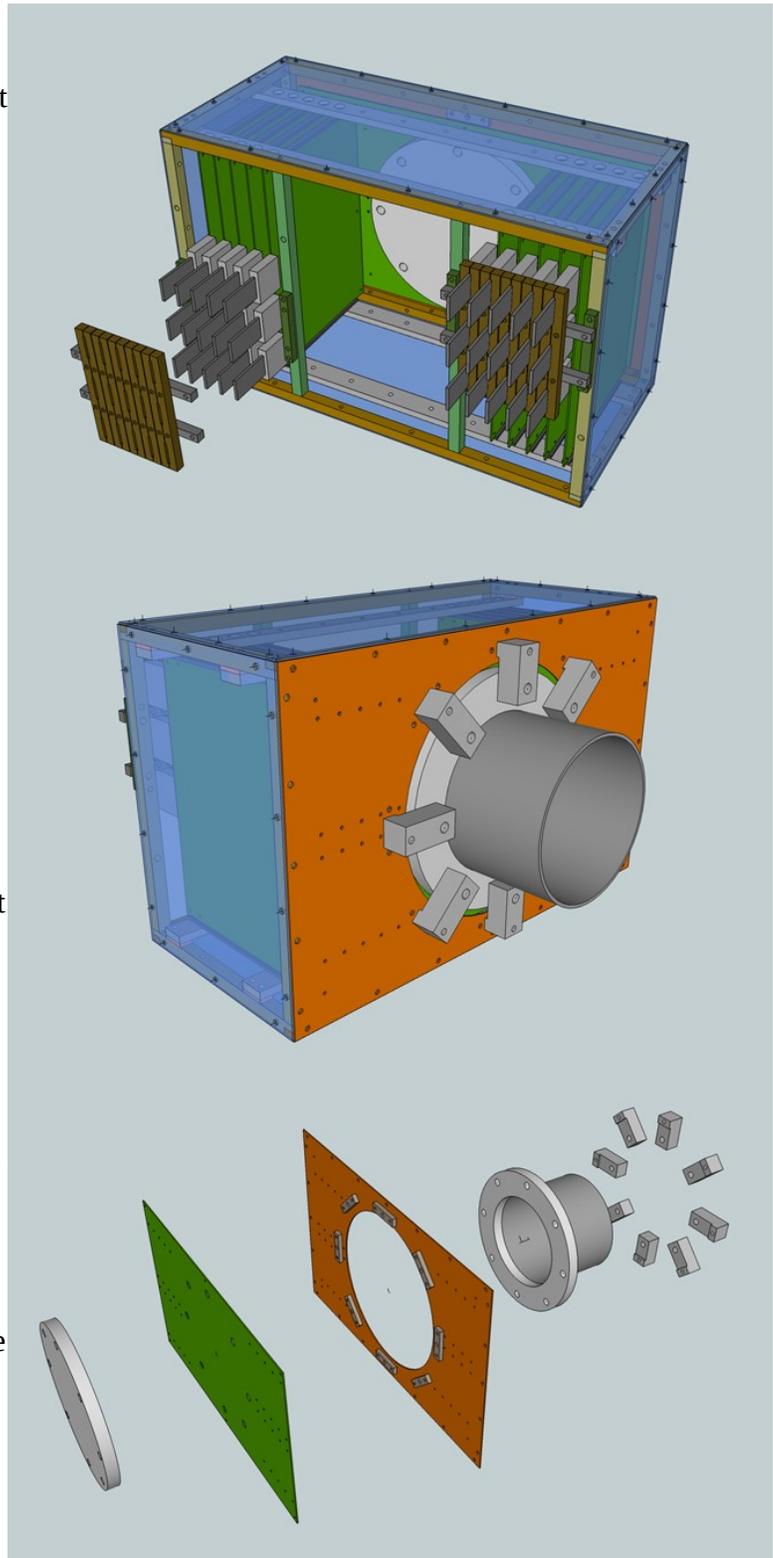
## 6. Cryostat feed through and mechanics

One design challenge for LArTPC technology is passing the power, control, and readout signals across the vacuum-tight cryostat barrier. In the ArgoNeuT experiment a large multilayer circuit board was developed to pass the 480 analog signals across this barrier. The ArgoNeuT feed-through PCB was sandwiched between an ASA style flange on the cryostat and an ASA-style flange cap and provided electrical connectivity between connectors on the inside and outside of the cryostat. The LArIAT setup required more power and control lines, necessitating a re-engineering of the feed through design.

The feed through (FT) card developed for LArIAT is sandwiched between an ASA flange and cap and is sealed with o-rings, just as with the previous ArgoNeuT feed through. However, the LArIAT FT card is supported with a stiff mechanical structure and backplane-style connectors. This design allows the WRD-48 cards to plug directly into the FT card. This arrangement facilitates assembly and repairs. Additionally, the direct connection of the WRD-48 cards to the FT card reduces the number of connections and cables relative to the ArgoNeuT precedent.

The LArIAT feed through card (FT card) is built as an 8-layer pcb with dimensions of 10 x 17 inches. The outer layers of the card are mostly uninterrupted ground planes to increase noise immunity. The internal traces are built with relatively large 12 mil design rules to enhance manufacturing yield and physical robustness. Signals on adjacent layers are staggered to reduce capacitive cross-talk couplings, and ground fills are provided wherever possible on all copper layers.

The connections from the FT card to the WRD-48 cards are through industry-standard VME-style DIN41612 connectors. The male side of the connectors is on the FT card, placing the female pins (which are more difficult to repair) on the more easily serviced WRD-48 cards. The connectors to the



WRD-48 cards are supported with conductive standoffs that make contact between the FT card ground planes and the solid copper sheet that forms the back of the WRD card cage. The FT card also provides the distribution of the three voltages supplied to each of the WRD-48 cards, simplifying the wiring and the WRD-48 front panel connections.

The FT card is supported by a mechanical structure that is rooted on the cryostat flange. The overall assembly of the FT card, the ten WRD-48 cards, and the WRD card cage is light enough to be safely cantilevered from the cryostat flange, which greatly simplifies the installation and eliminates the need for an external support framework. The back plate of the structure is a solid copper sheet which is electrical connected with the cryostat flange through lock washers and also connected to the FT card through 40 conductive standoffs. The copper plate and the cryostat flange are defined as the electrical ground of the TPC readout electronics.

The FT mechanical structure also contains a strain relief system that supports the 30 pleated foil cables that depart and head to the D2S rack. The strain relief system was designed with the highest emphasis on mechanical protection of the signal cabling and cards and thus a lesser emphasis on ease of use. This emphasis was chosen because of the mechanical dangers present in the crowded space at the top of the LArIAT cryostat. Due to this design compromise, the cables and card connections are very well protected from physical damage but it requires a full disassembly of the strain relief bars to be able to extract any WRD-48 card. The mechanics of the WRD card cage are shown in Figure 9.

## **7. Upgrade options**

The LArIAT front end electronics were designed with built-in flexibility. The Run 1 implementation made moderate use of the full diagnostic and monitoring potential of the system. This section describes a few different paths for upgrading the system for improved test signal capability, improved monitoring, a more adaptable digital control path, and remote power down options with granularity of individual WRD-48/CMB-48 card pairs.

### **7.1. ASIC test signals**

The ASIC test signal used in LArIAT Run 1 was the simple test pulser embedded on each WRD-48 card. This pulser is quite easy to use due to direct control from the Teensy and the DAQ system, and it served well in validating the proper function of all 480 TPC channels during commissioning. However, as it is currently implemented, the test pulse will fire on all ten WRD-48 cards at once. This makes it hard to interpret any cross-talk in the signals. A simple improvement to the system would be to distribute the test signal trigger logic to each WRD-48 card individually instead of fanning it out to all cards at once. A more ideal and general-purpose solution is to use a standalone commercial arbitrary waveform generator to give arbitrary pulse shapes and pulse amplitudes as the test signal. The most ideal system would be allow the test signal input to be selectively connected to any particular WRD-48 card.

### **7.2. Voltage and current monitoring**

The WRD-48 cards present several diagnostic monitor voltages at the front panel. The diagnostic values include the regulator output voltages both before and after a current-sensing resistor, and a voltage monitor line connected directly to the corresponding CMB-48 card. Additionally, the +/- 5 VDC supplies for the differential analog signal driver section are monitored. Thus a total of eight

diagnostic monitor voltages are presented at the front panel of each WRD-48 card.

These monitor voltages were only used during LArIAT Run 1 commissioning to trim the 1.8 volt regulators. As an upgrade to the system a voltage monitoring system could be implemented. Such a system would allow for monitoring during beam time. Also, since the there front panel ports for monitoring the VDD and VDDP directly on the CMB-48 cards, it would be possible to look at the noise conditions inside the cryostat during run time. The necessity of such a system is not clear, and the extra information might be a distraction in the control room. Nonetheless, it would be relatively straightforward to implement monitoring of the front-panel diagnostic voltages.

### **7.3. Digital Control Path**

The digital control lines for each CMB-48 card are presented on the front panel of each corresponding WRD-48 card. In the Run 1 configuration the CLK,CS,and RST lines are fanned out in parallel, while the SDI-SDO lines are daisy chained from one WRD-48 to the next. A finer-grained approach to the digital controls would be to replace the fanout of the CLK, CD, and RST lines and the SDI-SDO daisy chain with individual control lines leading to each WRD-48 card. The advantage would be that any particular WRD-48 card could be addressed independently of the rest of the system. This would allow, for instance, the setup of an automated recovery from any single-point failures occurring in the cryostat. However, the absence of any such failures during LArIAT Run 1 suggests that this reconfiguration of the digital controls may have little necessity.

### **7.4. Remote Power Down**

The WRD-48 cards also carry the ability to remotely power down the 1.8 VDC regulators through a front-panel port that provides access to the ENABLE inputs on the regulators. This line is internally held high through a 1k ohm resistance to +5 VDC. If this line is pulled low then the regulators will be disabled. This remote power-down function was not used during LArIAT Run 1. However, for diagnostic and noise-hunting procedures there is a clear utility in being able to selectively power down subsections of the TPC electronics. By using the WRD-48 front panel connections, any combination of the ten CMB-48 cards could be powered down remotely from the within DAQ architecture.

## **Appendix 1: Electronics design and software packages**

All of the cards in the LArIAT front end electronics system were designed using the open-source KiCAD software package (build BZR 4022). This software is under active development and is receiving development support from several groups including designers at CERN. Newer versions of KiCAD should be able to read the project files for the existing LArIAT designs, but in the case of any incompatibility it is advised to use KiCAD version “bzs 4022” (nicknamed “Old Stable”).

The KiCAD project files for the CMB-48, the Feed-through (FT) card, the WRD-48, and the D2S-64 should be found in the same directories as this manual. The resulting PCB production files (the Gerbers) and the BOMs can be found inside the KiCAD folders.

Additionally, the full set of schematics for the LArIAT front end boards should be included as a pdf files that accompany this document.

## **Appendix 2: Mechanical design software**

The mechanical designs for the LArIAT front end electronics hardware were modeled in the Sketchup software package from Trimble. Trimble offers a free viewer for Sketchup files. From this viewer all parts, dimensions, and the overall assembly can be read directly from the models. Alternatively, contact Dean Shooltz or Carl Bromberg for any specifics on the mechanical design. A full set of production drawings can be generated from the Sketchup files if requested.

## **Appendix 3: CMB-48 card design details**

The CMB-48 card holds 3 LArASIC version 4-Star front end amplifiers (ASICs). The card provides electrical connections to the LArIAT TPC wires and mechanical connection to the TPC structure. The CMB-48 board is located inside the cryostat and is thus very difficult or simply impossible to access during run time. The board is designed to minimize the sources of electrical noise, minimize the risk of failure due to thermal stresses, and to minimize the risk of failure due to component failures.

The board is designed for use in cryogenic conditions. For robustness under thermal stresses the number of vias was minimized, and all vias are present in redundant pairs. This reduces the risk of failures due to broken vias. The board was designed with 12 mil traces throughout. This relatively large trace width was chosen to reduce the risk of failures due to broken or damaged traces.

The circuitry includes input protection diodes and capacitive coupling of the wire plane input signals to the ASICs, arranged similarly to the design used in MicroBooNE. One difference from the MicroBooNE design is in the arrangement of the input protection diodes. In the MicroBooNE design the input protection diodes span between VDDP and ground, whereas in the LArIAT design the input diodes are connected only to VDDP. This means that in the LArIAT design the input traces are clamped to be within one diode drop of VDDP. This arrangement was chosen for three reasons. First, this arrangement of the protection diodes does not allow for any leakage current from VDDP to ground. Such a leakage current would be a source of electrical noise. Second, the arrangement of the diodes prevents any possibility of shorting VDDP to ground through failed diodes. Third, the diodes are connected to VDDP, since VDDP is the reference potential for the PMOS input circuitry in the ASICs.

The CMB-48 board was designed to minimize the distance between the wire plane signals and the LArASIC amplifiers. The LArASIC input section is PMOS, and thus referenced to VDDP. Because of this, the wire plane signals are routed over a VDDP plane for shielding.

The CMB-48 card is designed as a 4-layer circuit board, FR-4 based, overall dimensions 8.4 inches by 4.2 inches, with 1 oz copper specified on all layers. The board is specified with ENIG gold finish. The design uses surface-mount components on only the top layer. The layer stackup is as follows:

Layer 1: All analog signal traces and several of the digital interconnection traces. All surface-mount components are mounted to the top layer.

Layer 2: VDDP plane and ground plane. VDDP plane is under the wire plane input traces for shielding.

Layer 3: VDD plane, ground plane, and digital interconnects.

Layer 4: Ground plane, as complete as possible. The only interruptions are for via clearances.

The KiCad design files and the manufacturing files for the CMB-48 should be bundled with this documentation file.

#### **Appendix 4: WRD-48 card design details**

The WRD-48 cards are designed to be paired one-to-one with the CMB-48 cards inside the cryostat. The WRD-48 cards hold 48 channels of single-ended to differential analog amplifiers to transmit the TPC signals to the distant digitizers. These cards also provide low-noise power regulation, digital signal conditioning, front-panel diagnostic LEDs and voltage monitor ports, and an on-board test pulse generator. Adjustable crowbar circuits are present to provide protection to the electronics inside the cryostat. The WRD-48 cards are designed as four-layer FR-4 based circuit boards with 1 ounce copper on all layers. The design is primarily SMT with all parts on one side of the board.

The KiCad design files and the manufacturing files for the WRD-48 should be bundled with this documentation file.

#### **Appendix 5: D2S-64 card design details**

The D2S-64 cards serve the simple function of converting the differential analog signals from the WRD-48 cards to single-ended signals and driving these signals into the 50 ohm input impedance of the CAEN V1740 digitizers. The cards upstream of the D2S function are all 48-channel units (CMB-48 and WRD-48), whereas the CAEN digitizers are 64-channel units. The D2S cards are a natural place to regroup the signals into 64 channel units. This yields a one-to-one correspondence of D2S-64 cards to digitizer cards. A consequence of this layout is that only 7.5 D2S-64 cards are required for the complete system. The extra 32 channels on the unused half of one D2S-64 card in the system can be used as an embedded set of spare channels.

The KiCad design files and the manufacturing files for the D2S-64 should be bundled with this documentation file.

#### **Appendix 6: D2S-64 card crate design details**

A custom card crate was designed for the D2S-64 cards. The crate is designed to fit into any standard 19 inch equipment rack. The incoming signal cables enter at the rear of the chassis, where a support structure protects the cables and the board mount connectors from damage. As with the WRD-48 card chassis, this system was designed with the highest emphasis on the protection of the signal cabling and the cards and thus a lesser emphasis was placed on the ease of use. Due to this design compromise, the cables and cards are very well protected but it requires the removal of some of the cabling strain reliefs to facilitate removal of the D2S cards.

The power distribution and fuses for the D2S cards are located at the front of the crate. This allows for easy testing and replacing of fuses. Additionally, the power is connected to the D2S cards through front panel connections, which allows for unused cards to be easily taken offline.

## **Appendix 7: Signal cabling**

The environment inside the cryostat must be kept as clean as possible. This requirement led to the use of FEP-insulated (Fluorinated Ethylene Propylene) wiring for the ribbon cables running from the CMB-48 cards to the FT card. The FEP cabling is MOLEX part number F3001S-100-025-85. This is 100 line ribbon with solid 30 AWG silver plated conductors. The signals and ground connections are carried on 100 pin cabling terminated with 3M 82100 connectors at each end. The power supplies and digital controls are connected with 100 line cabling at the FT card side that is split to (5) 20 line units that run to the individual CMB-48 cards. This cabling is terminated with 3M 82100 connectors at the FT side and 3M 82020 connectors at the CMB-48 side.

The analog signals from the WRD-48 cards to the D2S-64 cards are carried on high-quality pleated foil cables with 3M brand MDR36 connectors. These cables were available from previous use in the ArgoNeuT experiment and provided LArIAT the option of using high quality cabling for the modest cost of the board-mount connectors. The board mount connectors are 3M model 10236-55H3PC (Digi-Key stock number 3M1821-ND).

The CAEN digitizers use high-density ribbon cable connectors at the signal inputs. The cables from the D2S-64 to the CAEN digitizers are modified versions of the the ribbon cables available from CAEN. The CAEN cables were ordered at 100 cm length and were cut in half to provide two 50 cm long sections. 3M model 80268 connectors were installed on the cut end of the cables to mate to the D2S-64 cards.

## **Appendix 8: Index of associated documentation**

The following documents should be found together:

1. The PDF file you are reading, as well as the LibreOffice source file
2. LArIAT-FE-Power.pdf, as well the powerpoint source file
3. Folder containing the CMB-48 PCB production files (named DS-1000)
4. Folder containing the WRD-48 PCB production files (named DS-1001AB)
5. Folder containing the Feed-through PCB production files (named DS-1002)
6. Folder containing the D2S-64 PCB production files (named DS-1003)
7. Folder containing the schematics showing the LArIAT-FE power distribution
8. Teensy program code listing or a pointer to the current version of this code
9. Channel mapping spreadsheet
10. WRD-48 front panel connections map as a pdf file.